3rd SEMESTER ELECTRONICS & TELECOMMUNICATION ENGINEERING

UNIT-1

BASICS OF DIGITAL ELECTRONICS

Introduction to Digital Electronics:

- Digital electronics deals with the electronic manipulation of numbers, or with the manipulation of varying quantities by means of numbers.
- Because it is convenient to do so, today's digital systems deal only with the numbers 'zero' and 'one', because they can be represented easily by 'off and 'on' within a circuit.
- This is not the limitation it might seem, for the binary system of counting can be used to represent any number that we can represent with the usual decimal (0 to 9) system that we use in everyday life.
- Digital Electronics is very important in today's life because if digital circuits compared to analog circuits are that signals represented digitally can be transmitted without degradation due to noise.

Advantages of Digital Circuits

- High accuracy and programmability
- Storage of digital data is easy
- Immune to noise
- Can be implemented in the form of integrated circuits (ICs)
- Greater reliability and flexibility

Disadvantages of Digital Circuits

- Expensive
- Operate on digital signals only
- Complex circuitry

Applications of Digital Circuits

- Mobile Phones, Calculators and Digital Computers
- Radios and communication Devices
- Signal Generator
- Smart Card
- Cathode Ray Oscilloscope (CRO)
- Analog to digital converters (ADC)
- Digital to analog converters (DAC), etc.

Number system:

- A number system is defined as a system of writing to express numbers.
- It is the mathematical notation for representing numbers of a given set by using digits or other symbols in a consistent manner.
- It provides a unique representation of every number and represents the arithmetic and algebraic structure of the figures.
- It also allows us to operate arithmetic operations like addition, subtraction and division. The value of any digit in a number can be determined by:
- The digit
- Its position in the number
- The base of the number system

Types of number system:

There are various types of number systems in mathematics. The four most common number system types are:

- Decimal number system (Base- 10)
- Binary number system (Base- 2)
- Octal number system (Base-8)

- Hexadecimal number system (Base- 16) A number N in base or radix 'r' can be written as:

$(N)_b = d_{n-1}\ d_{n-2}$ -- -- -- -- $d_1\ d_0\ .\ d_{-1}\ d_{-2}$---------- d_{-m}

In the above, dn-1 to d0 is the integer part, then follows a radix point, and then d-1 to d-m is the fractional part.

D_{n-1} = Most significant bit (MSB) d_{-m}

= Least significant bit (LSB)

Decimal number system:

The base or radix of Decimal number system is 10. So, the numbers ranging from 0 to 9 are used in this number system. Mathematically, we can write it as

$1358.246 = (1 \times 10^3) + (3 \times 10^2) + (5 \times 10^1) + (8 \times 10^0) + (2 \times 10^{-1}) + (4 \times 10^{-2}) + (6 \times 10^{-3})$

Binary number system:

All digital circuits and systems use this binary number system. The base or radix of this number system is 2. So, the numbers 0 and 1 are used in this number system.

Mathematically, we can write it as

$1101.011 = (1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0) + (0 \times 2^{-1}) + (1 \times 2^{-2}) + (1 \times 2^{-3})$

Octal number system:

The base or radix of octal number system is 8. So, the numbers ranging from 0 to 7 are used in this number system.

Mathematically, we can write it as

$1457.236 = (1 \times 8^3) + (4 \times 8^2) + (5 \times 8^1) + (7 \times 8^0) + (2 \times 8^{-1}) + (3 \times 8^{-2}) + (6 \times 8^{-3})$

Hexadecimal number system:

The base or radix of Hexa-decimal number system is 16. So, the numbers ranging from 0 to 9 and the letters from A to F are used in this number system. The decimal equivalent of Hexadecimal digits from A to F are 10 to 15.

Mathematically, we can write it as

$1A05.2C4 = (1 \times 16^3) + (10 \times 16^2) + (0 \times 16^1) + (5 \times 16^0) + (2 \times 16^{-1}) + (12 \times 16^{-2}) + (4 \times 16^{-3})$

Conversion from one system to another number system:

Decimal number system to other number system:

If the decimal number contains both integer part and fractional part, then convert both the parts of decimal number into another base individually. Steps for converting the decimal number into its equivalent number of any base 'r'-

- Do division of integer part of decimal number and **successive quotients** with base 'r' and note down the remainders till the quotient is zero. Consider the remainders in reverse order to get the integer part of equivalent number of base 'r'. That means, first and last remainders denote the least significant digit and most significant digit respectively.
- Do multiplication of fractional part of decimal number and **successive fractions** with base 'r' and note down the carry till the result is zero or the desired number of equivalent digits is obtained. Consider the normal sequence of carry in order to get the fractional part of equivalent number of base 'r'.

Decimal to binary:

Example- $(152.25)_{10}$ Step 1:

Divide the number 152 and its successive quotients with base 2.

Operation	Quotient	Remainder

152/2	76	0 (LSB)
76/2	38	0
38/2	19	0
19/2	9	1
9/2	4	1
4/2	2	0
2/2	1	0
1/2	0	1(MSB)

$(152)_{10} = (10011000)_2$ Step 2:

Now, perform the multiplication of 0.27 and successive fraction with base 2.

Operation	Result	carry
0.25×2	0.50	0
0.50×2	0	1

$(0.25)_{10} = (.01)_2$

Decimal to octal:

Example- $(152.25)_{10}$Step 1:

Divide the number 152 and its successive quotients with base 8.

Operation	Quotient	Remainder
152/8	19	0
19/8	2	3
2/8	0	2

$(152)_{10} = (230)_8$

Step 2:

Now perform the multiplication of 0.25 and successive fraction with base 8.

Operation	Result	carry
0.25×8	**0**	**2**

$(0.25)_{10}=(2)_8$

So, the octal number of the decimal number 152.25 is **230.2 Decimal to hexadecimal:**

Example- $(152.25)_{10}$ Step 1:

Divide the number 152 and its successive quotients with base 8.

Operation	Quotient	Remainder
152/16	9	8
9/16	0	9

$(152)_{10} = (98)_{16}$

Step 2:

Now perform the multiplication of 0.25 and successive fraction with base 16.

Operation	Result	carry
0.25×16	0	4

$(0.25)_{10} = (4)_{16}$

So, the hexadecimal number of the decimal number 152.25 is **230.4. Binary to other number system:**

Binary to decimal:

The process starts from multiplying the bits of binary number with its corresponding positional weights. And lastly, we add all those products.

Example- $(10110.001)_2$

$(10110.001)_2$ $=(1\times2^4)+(0\times2^3)+(1\times2^2)+(1\times2^1)+(0\times2^0)+(0\times2^{-1})+(0\times2^{-2})+(1\times2^{-3})$

$(10110.001)_2$ $=(1\times16)+(0\times8)+(1\times4)+(1\times2)+(0\times1)+(0\times12)+(0\times14)+(1\times18)$

$(10110.001)_2$ $=16+0+4+2+0+0+0+0.125$

$(10110.001)_2$ $=$**$(22.125)_{10}$** **Binary to octal:**

In a binary number, the pair of three bits is equal to one octal digit. Two steps to convert a binary number into an octal number which are as follows:

- In the first step, we have to make the pairs of three bits on both sides of the binary point. If there will be one or two bits left in a pair of three bits pair, we add the required number of zeros on extreme sides.
- In the second step, we write the octal digits corresponding to each pair. **Example- $(111110101011.0011)_2$**

1. Firstly, we make pairs of three bits on both sides of the binary point. 111
110 101 011.001 1
On the right side of the binary point, the last pair has only one bit. To make it a complete pair of three bits, we added two zeros on the extreme side.
111 110 101 011.001 100 2. Then, we wrote the octal digits, which correspond to each pair.
$(111110101011.0011)_2 = (7653.14)_8$ Binary to hexadecimal:

The base numbers of binary and hexadecimal are 2 and 16, respectively. In a binary number, the pair of four bits is equal to one hexadecimal digit. There are also only two steps to convert a binary number into a hexadecimal number which are as follows:

1. In the first step, we have to make the pairs of four bits on both sides of the binary point. If there will be one, two, or three bits left in a pair of four bits pair, we add the required number of zeros on extreme sides.
2. In the second step, we write the hexadecimal digits corresponding to each pair.

Example- $(10110101011.0011)_2$

1. Firstly, we make pairs of four bits on both sides of the binary point.
111 1010 1011.0011
On the left side of the binary point, the first pair has three bits. To make it a complete pair of four bits, add one zero on the extreme side.
0111 1010 1011.0011
2. Then, we write the hexadecimal digits, which correspond to each pair.
$(011110101011.0011)_2 = (7AB.3)_{16}$ Octal to other number system:

Octal to decimal:

The process starts from multiplying the digits of octal numbers with its corresponding positional weights. And lastly, we add all those products.

Example- $(152.25)_8$ Step 1:

We multiply each digit of **152.25** with its respective positional weight, and last, we add the products of all the bits with its weight.

$(152.25)_8 = (1\times8^2)+(5\times8^1)+(2\times8^0)+(2\times8^{-1})+(5\times8^{-2})$
$(152.25)_8 = 64+40+2+(2\times18)+(5\times164)$
$(152.25)_8 = 64+40+2+0.25+0.078125$
$(152.25)_8 = 106.328125$

So, the decimal number of the octal number 152.25 is **106.328125** **Octal to binary:**

The process of converting octal to binary is the reverse process of binary to octal. We write the three bits binary code of each octal number digit. **Example- $(152.25)_8$**

We write the three-bit binary digit for 1, 5, 2, and 5.

$(152.25)_8$ = $(001101010.010101)_2$

So, the binary number of the octal number 152.25 is **$(001101010.010101)_2$** **Octal to hexadecimal:**

For converting octal to hexadecimal, there are two steps required to perform, which are as follows:

1. In the first step, we will find the binary equivalent of number.
2. Next, we have to make the pairs of four bits on both sides of the binary point. If there will be one, two, or three bits left in a pair of four bits pair, we add the required number of

zeros on extreme sides and write the hexadecimal digits corresponding to each pair.

Example- $(152.25)_8$Step 1:

We write the three-bit binary digit for 1, 5, 2, and 5.

$(152.25)_8$ $=(001101010.010101)_2$

So, the binary number of the octal number 152.25 is **$(001101010.010101)_2$Step 2:**

1. Now, we make pairs of four bits on both sides of the binary point.

0 0110 1010.0101 01

On the left side of the binary point, the first pair has only one digit, and on the right side, the last pair has only two-digit. To make them complete pairs of four bits, add zeros on extreme sides.

0000 0110 1010.0101 0100

2. Now, we write the hexadecimal digits, which correspond to each pair.

$(0000\ 0110\ 1010.0101\ 0100)_2$ = $(6A.54)_{16}$

Hexadecimal to other number system:

Hexadecimal to decimal:

The process of converting hexadecimal to decimal is the same as binary to decimal. The process starts from multiplying the digits of hexadecimal numbers with its corresponding positional weights. And lastly, we add all those products.

Let's take an example to understand how the conversion is done from hexadecimal to decimal.

Example- $(152A.25)_{16}$Step 1:

We multiply each digit of **152A.25** with its respective positional weight, and last we add the products of all the bits with its weight.

$(152A.25)_{16}$ $=(1\times16^3)+(5\times16^2)+(2\times16^1)+(A\times16^0)+(2\times16^{-1})+(5\times16^{-2})$

$(152A.25)_{16}$ $=(1\times4096)+(5\times256)+(2\times16)+(10\times1)+(2\times16^{-1})+(5\times16^{-2})$

$(152A.25)_{16}$ $=4096+1280+32+10+(2\times1/16)+(5\times1256)$

$(152A.25)_{16}$ $=5418+0.125+0.125$

$(152A.25)_{16}$ $=5418.14453125$

So, the decimal number of the hexadecimal number 152A.25 is **5418.14453125Hexadecimal to binary:**

The process of converting hexadecimal to binary is the reverse process of binary to hexadecimal. We write the four bits binary code of each hexadecimal number digit. **Example - $(152A.25)_{16}$**

We write the four-bit binary digit for 1, 5, A, 2, and 5.

$(152A.25)_{16} = (0001\ 0101\ 0010\ 1010.0010\ 0101)_2$

So, the binary number of the hexadecimal number 152.25 is **$(1010100101010.00100101)_2$**

Binary equivalent	Hexadecimal
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Hexadecimal to octal:

For converting hexadecimal to octal, there are two steps required to perform, which are as follows:

1. In the first step, we will find the binary equivalent of the hexadecimal number.
2. Next, we have to make the pairs of three bits on both sides of the binary point. If there will be one or two bits left in a pair of three bits pair, we add the required number of zeros on extreme sides and write the octal digits corresponding to each pair.

Example- $(152A.25)_{16}$Step 1:

We write the four-bit binary digit for 1, 5, 2, A, and 5.

$(152A.25)_{16} = (0001\ 0101\ 0010\ 1010.0010\ 0101)_2$

So, the binary number of hexadecimal number 152A.25 is **$(0011010101010.010101)_2$Step 2:**

3. Then, we make pairs of three bits on both sides of the binary point.

001 010 100 101 010.001 001 010

4. Then, we write the octal digit, which corresponds to each pair.

$(001010100101010.001001010)_2 = (12452.112)_8$

So, the octal number of the hexadecimal number 152A.25 is **12452.112**

Arithmetic operation:

Two types of operation that are performed on binary data include arithmetic and logic operations. Basic arithmetic operations include addition, subtraction, multiplication and division.

Binary addition:

There are four rules for binary addition:

Input A	Input B	Sum (S) A+B	Carry (C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Example-

0011010 + 001100 = 00100110

	1 1	carry
	0 0 1 1 0 1 0	$= 26_{10}$
+	0 0 0 1 1 0 0	$= 12_{10}$
	0 1 0 0 1 1 0	$= 38_{10}$

Binary subtraction:

There are four rules for binary subtraction:

Input A	Input B	Subtract (S) A-B	Borrow (B)
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

Example-

0011010 - 001100 = 00001110

	1 1	borrow
	0 0 ~~1 1~~ 0 1 0	$= 26_{10}$
-	0 0 0 1 1 0 0	$= 12_{10}$
	0 0 0 1 1 1 0	$= 14_{10}$

Binary multiplication:

There are four rules of binary multiplication.

Input A	Input B	Multiply (M) AxB
0	0	0
0	1	0
1	0	0
1	1	1

Example:

0011010 x 001100 = 100111000

	0 0 1 1 0 1 0	$= 26_{10}$
x	0 0 0 1 1 0 0	$= 12_{10}$
	0 0 0 0 0 0 0	
	0 0 0 0 0 0 0	
	0 0 1 1 0 1 0	
	0 0 1 1 0 1 0	
	0 1 0 0 1 1 1 0 0 0	$= 312_{10}$

Binary division:

There are four parts in any division: Dividend, Divisor, quotient, and remainder.

Input A	Input B	Divide (D) A/B
0	0	Not defined
0	1	0
1	0	Not defined
1	1	1

Example-

101010 / 000110 = 000111

```
                  1 1 1      = 7₁₀
          ------------------
000110 ) 1 0 1 0 1 0         = 42₁₀
       - 1 1 0               = 6₁₀
       -------
         1 0 0 1
       - 1 1 0
       -------
           1 1 0
         - 1 1 0
         -------
               0
```

Signed binary number representation:

- In mathematics, positive numbers (including zero) are represented as unsigned numbers.
- That is, we do not put the +ve sign in front of them to show that they are positive numbers.
- However, when dealing with negative numbers we do use a -ve sign in front of the number to show that the number is negative in value and different from a positive unsigned value, and the same is true with signed binary numbers.
- However, in digital circuits there is no provision made to put a plus or even a minus sign to a number, since digital systems operate with binary numbers that are represented in terms of "0's" and "1's".
- For signed binary numbers the most significant bit (MSB) is used as the sign bit.
- If the sign bit is "0", this means the number is positive in value.
- If the sign bit is "1", then the number is negative in value.

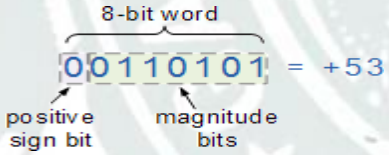
3 ways to represent negative binary number-

1. Sign magnitude
2. 1's compliment
3. 2' compliment **Sign magnitude:**

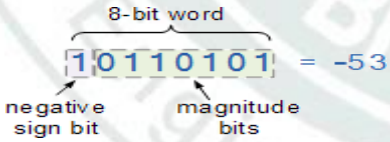
Left most digit is used to indicate the sign and the remaining digits the magnitude or value of the number.

Example-

Positive sign magnitude:



Negative sign magnitude:



The disadvantage here is that whereas before we had a full range n-bit unsigned binary number, we now have an n-1 bit signed binary number giving a reduced range of digits from:

$$-2^{(n-1)} \text{ to } +2^{(n-1)}$$

1's complement:

- The one's complement of a negative binary number is the complement of its positive counterpart.
- Thus, the one's complement of "1" is "0" and vice versa, then the one's complement of 100101002 is simply 011010112 as all the 1's are changed to 0's and the 0's to 1's.

For representing the positive numbers, there is nothing to do.

- But for representing negative numbers, we have to use 1's complement technique.
- For representing the negative number, we first have to represent it with a positive sign, and then we find the 1's complement of it.

Example- 11010.1101

For finding 1's complement of the given number, change all 0's to 1 and all 1's to 0. So, the 1's complement of the number 11010.1101 comes out 00101.0010. **2's complement:**

- 2's complement is also used to represent the signed binary numbers.
- For finding 2's complement of the binary number, we will first find the 1's complement of the binary number and then add 1 to the least significant bit of it.

Example- 110100

For finding 2's complement of the given number, change all 0's to 1 and all 1's to 0. So, the 1's complement of the number 110100 is 001011. Now add 1 to the LSB of this number, i.e., (001011)+1=001100.

Addition and subtraction using 1's complement:

There are three different cases possible when we add two binary numbers which are as follows:

Case 1: Addition of the positive number with a negative number when the positive number has a greater magnitude.

Initially, calculate the 1's complement of the given negative number. Sum up with the given positive number. If we get the end-around carry 1, it gets added to the LSB.

Example: 1101 and -1001

- First, find the 1's complement of the negative number 1001. So, for finding 1's complement, change all 0 to 1 and all 1 to 0. The 1's complement of the number 1001 is 0110.
- Now, add both the numbers, i.e., 1101 and 0110; 1101+0110=1 0011
- By adding both numbers, we get the end-around carry 1. We add this end around carry to the LSB of 0011.

  0011+1=0100

Case 2: Adding a positive value with a negative value in case the negative number has a higher magnitude.

Initially, calculate the 1's complement of the negative value. Sum it with a positive number. In this case, we did not get the end-around carry. So, take the 1's complement of the result to get the final result.

Note: The resultant is a negative value.

Example: 1101 and -1110

- First find the 1's complement of the negative number 1110. So, for finding 1's complement, we change all 0 to 1, and all 1 to 0. 1's complement of the number 1110 is 0001.
- Now, add both the numbers, i.e., 1101 and 0001; 1101+0001= 1110
- Now, find the 1's complement of the result 1110 that is the final result. So, the 1's complement of the result 1110 is 0001, and we add a negative sign before the number so that we can identify that it is a negative number.

Case 3: Addition of two negative numbers

In this case, first find the 1's complement of both the negative numbers, and then we add both these complement numbers. In this case, we always get the end-around carry, which get added to the LSB, and for getting the final result, we take the 1's complement of the result.

Note: The resultant is a negative value.

Example: -1101 and -1110 in five-bit register

- Firstly, find the 1's complement of the negative numbers 01101 and 01110. So, for finding 1's complement, we change all 0 to 1, and all 1 to 0. 1's complement of the number 01110 is 10001, and 01101 is 10010.

- Now, we add both the complement numbers, i.e., 10001 and 10010; 10001+10010= 1 00011
- By adding both numbers, we get the end-around carry 1. We add this end-around carry to the LSB of 00011.
  00011+1=00100
- Now, find the 1's complement of the result 00100 that is the final answer. So, the 1's complement of the result 00100 is 110111, and add a negative sign before the number so that we can identify that it is a negative number.

Addition and subtraction using 2's complement:

There are three different cases possible when we add two binary numbers using 2's complement, which is as follows:

Case 1: Addition of the positive number with a negative number when the positive number has a greater magnitude.

Initially find the 2's complement of the given negative number. Sum up with the given positive number. If we get the end-around carry 1 then the number will be a positive number and the carry bit will be discarded and remaining bits are the final result.

Example: 1101 and -1001

- First, find the 2's complement of the negative number 1001. So, for finding 2's complement, change all 0 to 1 and all 1 to 0 or find the 1's complement of the number 1001. The 1's complement of the number 1001 is 0110, and add 1 to the LSB of the result 0110. So the 2's complement of number 1001 is 0110+1=0111
- Add both the numbers, i.e., 1101 and 0111;
  1101+0111=1 0100
- By adding both numbers, we get the end-around carry 1. We discard the end-around carry. So, the addition of both numbers is 0100.

Case 2: Adding of the positive value with a negative value when the negative number has a higher magnitude.

Initially, add a positive value with the 2's complement value of the negative number. Here, no end-around carry is found. So, we take the 2's complement of the result to get the final result.

Note: The resultant is a negative value.

Example: 1101 and -1110

- First, find the 2's complement of the negative number 1110. So, for finding 2's complement, add 1 to the LSB of its 1's complement value 0001.
  0001+1=0010
- Add both the numbers, i.e., 1101 and 0010; 1101+0010= 1111
- Find the 2's complement of the result 1110 that is the final result. So, the 2's complement of the result 1110 is 0001, and add a negative sign before the number so that we can identify that it is a negative number.

Case 3: Addition of two negative numbers

In this case, first, find the 2's complement of both the negative numbers, and then we will add both these complement numbers. In this case, we will always get the end-around carry, which will be added to the LSB, and forgetting the final result, we will take the2's complement of the result.

Note: The resultant is a negative value.

Example: -1101 and -1110 in five-bit register

- Firstly, find the 2's complement of the negative numbers 01101 and 01110. So, for finding 2's complement, we add 1 to the LSB of the 1's complement of these numbers. 2's complement of the number 01110 is 10010, and 01101 is 10011.
- We add both the complement numbers, i.e., 10001 and 10010; 10010+10011= 1 00101

- By adding both numbers, we get the end-around carry 1. This carry is discarded and the final result is the 2.s complement of the result 00101. So, the 2's complement of the result 00101 is 11011, and we add a negative sign before the number so that we can identify that it is a negative number.

Digital codes:

In the coding, when numbers or letters are represented by a specific group of symbols, it is said to be that number or letter is being encoded. The group of symbols is called as code. The digital data is represented, stored and transmitted as group of bits. This group of bits is also called as binary code.

Advantages of Binary Code:

- Binary codes are suitable for the computer applications.
- Binary codes are suitable for the digital communications.
- Binary codes make the analysis and designing of digital circuits if we use the binary codes.
- Since only 0 & 1 are being used, implementation becomes easy.

Classification of binary codes:

The codes are broadly categorized into following four categories.

- Weighted Codes
- Non-Weighted Codes
- Binary Coded Decimal Code
- Alphanumeric Codes
- Error Detecting Codes
- Error Correcting Codes **Weighted Codes:**

Weighted binary codes are those binary codes which obey the positional weight principle. Each position of the number represents a specific weight. Several systems of the codes are used to express the decimal digits 0 through 9. In these codes each decimal digit is represented by a group of four bits.

Decimal Digit	8421 Code	2421 Code	84-2-1 Code
0	0000	0000	0000
1	0001	0001	0111
2	0010	0010	0110
3	0011	0011	0101
4	0100	0100	0100
5	0101	1011	1011

6	0110	1100	1010
7	0111	1101	1001
8	1000	1110	1000
9	1001	1111	1111

8 4 2 1 code

- The weights of this code are 8, 4, 2 and 1.
- This code has all positive weights. So, it is a **positively weighted code**.
- This code is also called as **natural BCDBinary Coded Decimalcode**.
- In this code each decimal digit is represented by a 4-bit binary number.
- BCD is a way to express each of the decimal digits with a binary code.
- In the BCD, with four bits we can represent sixteen numbers (0000 to 1111).
- But in BCD code only first ten of these are used (0000 to 1001).
- The remaining six code combinations i.e., 1010 to 1111 are invalid in BCD.

Decimal	0	1	2	3	4	5	6	7	8	9
BCD	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001

Example

Let us find the BCD equivalent of the decimal number 786. This number has 3 decimal digits 7, 8 and 6. From the table, we can write the BCD 84218421 codes of 7, 8 and 6 are 0111, 1000 and 0110 respectively.

$$786_{10} = 0111\ 1000\ 0110_{BCD}$$

There are 12 bits in BCD representation, since each BCD code of decimal digit has 4 bits.

Advantages of BCD Codes

- It is very similar to decimal system.
- We need to remember binary equivalent of decimal numbers 0 to 9 only.

Disadvantages of BCD Codes

- The addition and subtraction of BCD have different rules.
- The BCD arithmetic is little more complicated.
- BCD needs more number of bits than binary to represent the decimal number. So, BCD is less efficient than binary.

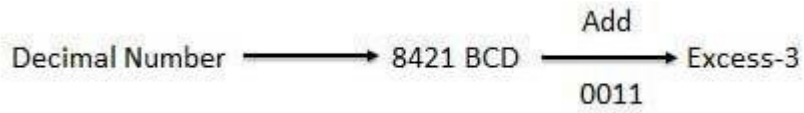
Non-weighted code:

n this type of binary codes, the positional weights are not assigned. The examples of nonweighted codes are Excess-3 code and Gray code.

Excess-3 code

- The Excess-3 code is also called as XS-3 code.
- It is non-weighted code used to express decimal numbers.

- The Excess-3 code words are derived from the 8421 BCD code words adding (0011)2 or (3)10 to each code word in 8421.
- The excess-3 codes are obtained as follows –



Decimal	BCD 8 4 2 1	Excess-3 BCD + 0011
0	0 0 0 0	0 0 1 1
1	0 0 0 1	0 1 0 0
2	0 0 1 0	0 1 0 1
3	0 0 1 1	0 1 1 0
4	0 1 0 0	0 1 1 1
5	0 1 0 1	1 0 0 0
6	0 1 1 0	1 0 0 1
7	0 1 1 1	1 0 1 0
8	1 0 0 0	1 0 1 1
9	1 0 0 1	1 1 0 0

Gray Code

- It is the non-weighted code and it is not arithmetic codes.
- That means there are no specific weights assigned to the bit position.
- It has a very special feature that, only one bit will change each time the decimal number is incremented as shown in fig.
- As only one-bit changes at a time, the gray code is called as a unit distance code.
- The gray code is a cyclic code. Gray code cannot be used for arithmetic operation.

Decimal	BCD	Gray
0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1
2	0 0 1 0	0 0 1 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 1 1 0
5	0 1 0 1	0 1 1 1
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 0 0
8	1 0 0 0	1 1 0 0
9	1 0 0 1	1 1 0 1

Binary code to Gray Code Conversion:

- Consider the given binary code and place the MSB of binary to the left of MSB.

- Compare the successive two bits starting from MSB. If the 2 bits are same, then the output is zero. Otherwise, output is one.
- Repeat the above step till the LSB of Gray code is obtained.

Example-

From the table, we know that the Gray code corresponding to binary code 1000 is 1100. Now, let us verify it by using the above procedure. Given, binary code is 1000. Step 1 − By placing same MSB to the left of MSB, the binary code will be 1000.

Step 2 − By comparing successive two bits of new binary code, we will get the gray code as 1100.

Application of Gray code:

- Gray code is popularly used in the shaft position encoders.
- A shaft position encoder produces a code word which represents the angular position of the shaft.

Alphanumeric codes:

- A binary digit or bit can represent only two symbols as it has only two states '0' or '1'.
- But this is not enough for communication between two computers because there we need many more symbols for communication.
- These symbols are required to represent 26 alphabets with capital and small letters, numbers from 0 to 9, punctuation marks and other symbols.
- The alphanumeric codes are the codes that represent numbers and alphabetic characters.
- Mostly such codes also represent other characters such as symbol and various instructions necessary for conveying information.
- An alphanumeric code should at least represent 10 digits and 26 letters of alphabet i.e. total 36 items.
- The following two alphanumeric codes are very commonly used for the data representation.

    i. American Standard Code for Information Interchange (ASCII).
    ii. Extended Binary Coded Decimal Interchange Code (EBCDIC).
- ASCII code is a 7-bit code whereas EBCDIC is an 8-bit code.
- ASCII code is more commonly used worldwide while EBCDIC is used primarily in large IBM computers.

Error detection codes:

- Error detection codes are used to detect the errors present in the received data bitstream.
- These codes contain some bits, which are included appended to the original bit stream.
- These codes detect the error, if it is occurred during transmission of the original data bitstream.
- Example − Parity code, Hamming code.

Error correction codes:

- Error correction codes are used to correct the errors present in the received data bitstream so that, we will get the original data.
- Error correction codes also use the similar strategy of error detection codes.
- Example − Hamming code.

Therefore, to detect and correct the errors, additional bits are appended to the data bits at the time of transmission. **Logic gates:**

- Logic gates play an important role in circuit design and digital systems.
- It is a building block of a digital system and an electronic circuit that always have only one output.

- These gates can have one input or more than one input, but most of the gates have two inputs.

We can classify these Logic gates into the following three categories.

1. Basic gates
2. Universal gates
3. Special gates **Basic gates:**

The basic gates are AND, OR & NOT gates.

AND gate:

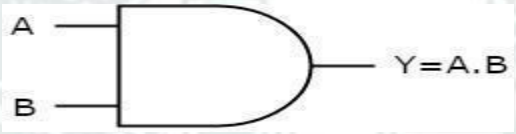
An AND gate is a digital circuit that has two or more inputs and produces an output, which is the **logical AND** of all those inputs. It is optional to represent the **Logical AND** with the symbol '.'.

The following table shows the **truth table** of 2-input AND gate.

A	B	Y = A.B
0	0	0
0	1	0
1	0	0
1	1	1

Here A, B are the inputs and Y is the output of two input AND gate. If both inputs are '1', then only the output, Y is '1'. For remaining combinations of inputs, the output, Y is '0'.

The following figure shows the **symbol** of an AND gate, which is having two inputs A, B and one output, Y.



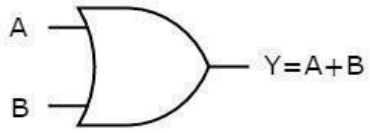
OR gate:

An OR gate is a digital circuit that has two or more inputs and produces an output, which is the logical OR of all those inputs. This **logical OR** is represented with the symbol '+'. The following table shows the **truth table** of 2-input OR gate.

A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1

Here A, B are the inputs and Y is the output of two input OR gate. If both inputs are '0', then only the output, Y is '0'. For remaining combinations of inputs, the output, Y is '1'.

The following figure shows the **symbol** of an OR gate, which is having two inputs A, B and one output, Y.



This OR gate produces an output Y, which is the **logical OR** of two inputs A, B.

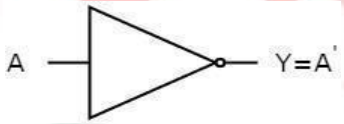
NOT gate:

A NOT gate is a digital circuit that has single input and single output. The output of NOT gate is the **logical inversion** of input. Hence, the NOT gate is also called as inverter. The following table shows the **truth table** of NOT gate.

A	Y = A'
0	1
1	0

Here A and Y are the input and output of NOT gate respectively. If the input, A is '0', then the output, Y is '1'. Similarly, if the input, A is '1', then the output, Y is '0'.

The following figure shows the **symbol** of NOT gate, which is having one input, A and one output, Y.



This NOT gate produces an output Y, which is the **complement** of input, A.

Universal gates

NAND & NOR gates are called as **universal gates**.

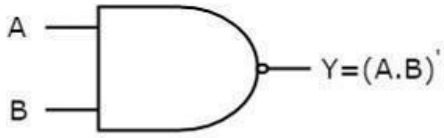
NAND gate

NAND gate is a digital circuit that has two or more inputs and produces an output, which is the **inversion of logical AND** of all those inputs.

The following table shows the **truth table** of 2-input NAND gate.

A	B	Y = (A.B)'
0	0	1
0	1	1
1	0	1
1	1	0

The following image shows the **symbol** of NAND gate, which is having two inputs A, B and one output, Y.



NAND gate operation is same as that of AND gate followed by an inverter. That's why the NAND gate symbol is represented like that.

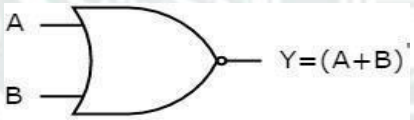
NOR gate:

NOR gate is a digital circuit that has two or more inputs and produces an output, which is the **inversion of logical OR** of all those inputs.

The following table shows the **truth table** of 2-input NOR gate

A	B	Y = (A+B)'
0	0	1
0	1	0
1	0	0
1	1	0

The following figure shows the **symbol** of NOR gate, which is having two inputs A, B and one output, Y.



NOR gate operation is same as that of OR gate followed by an inverter. That's why the NOR gate symbol is represented like that.

Special Gates

Ex-OR & Ex-NOR gates are called as special gates. Because, these two gates are special cases of OR & NOR gates.

Ex-OR gate:

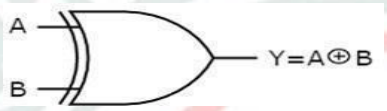
The full form of Ex-OR gate is **Exclusive-OR** gate. Its function is same as that of OR gate except for some cases, when the inputs having even number of ones. The following table shows the **truth table** of 2-input Ex-OR gate.

A	B	Y = A⊕B

0	0	0
0	1	1
1	0	1
1	1	0

The output of Ex-OR gate is '1', when only one of the two inputs is '1'. And it is zero, when both inputs are same.

Below figure shows the **symbol** of Ex-OR gate, which is having two inputs A, B and one output, Y.



The output of Ex-OR gate is '1', when odd number of ones present at the inputs. Hence, the output of Ex-OR gate is also called as an **odd function**.

Ex-NOR gate:

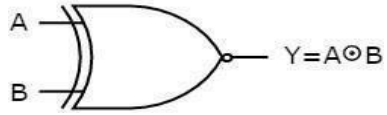
The full form of Ex-NOR gate is **Exclusive-NOR** gate. Its function is same as that of NOR gate except for some cases, when the inputs having even number of ones.

The following table shows the **truth table** of 2-input Ex-NOR gate.

A	**B**	**Y = A⊙B**
0	0	1
0	1	0
1	0	0
1	1	1

The output of Ex-NOR gate is '1', when both inputs are same. And it is zero, when both the inputs are different.

The following figure shows the **symbol** of Ex-NOR gate, which is having two inputs A, B and one output, Y.

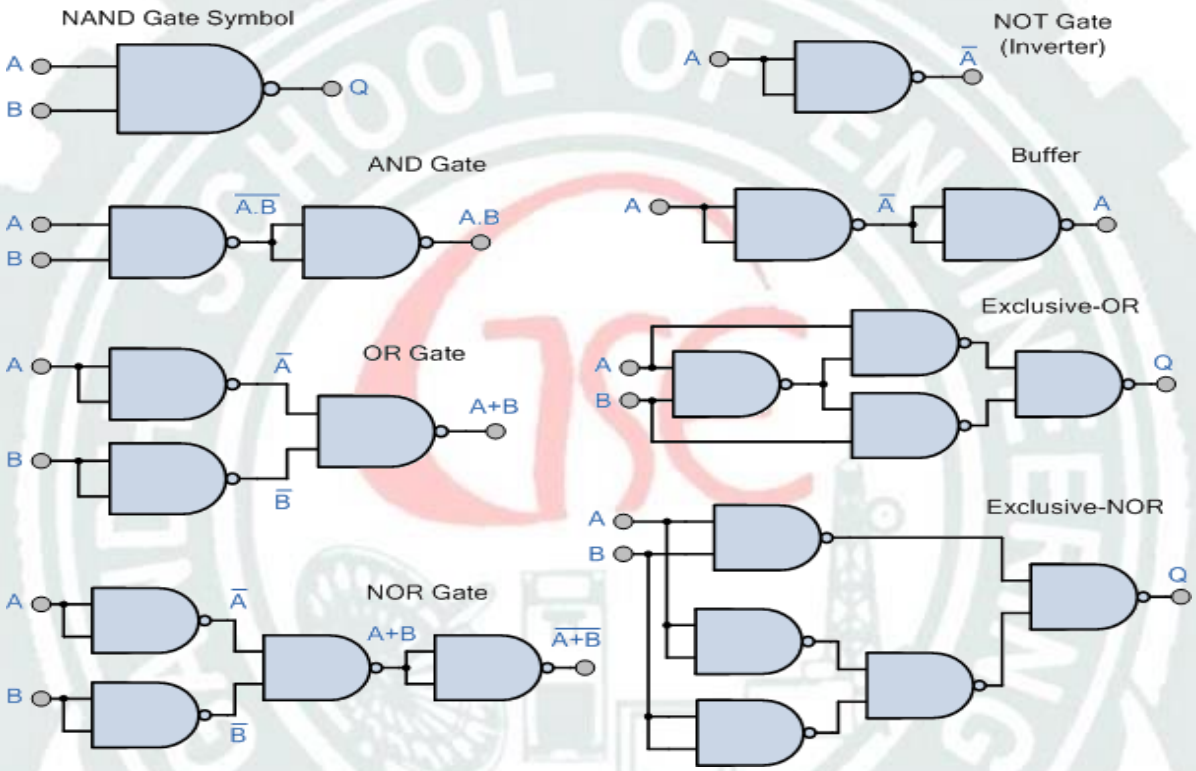


The output of Ex-NOR gate is '1', when even number of ones present at the inputs. Hence, the output of Ex-NOR gate is also called as an **even function**.

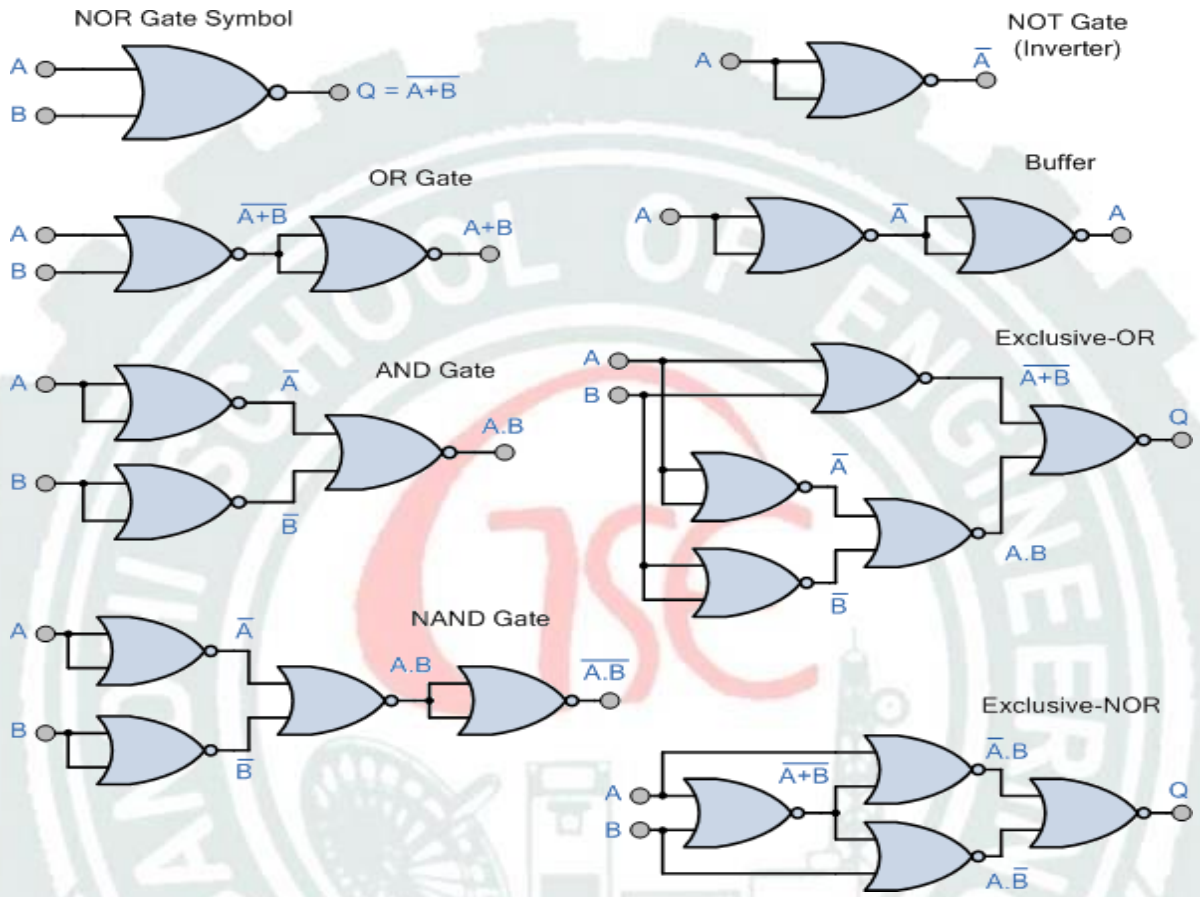
From the above truth tables of Ex-OR & Ex-NOR logic gates, we can easily notice that the Ex-NOR operation is just the logical inversion of Ex-OR operation.

Universal gates and its realization:

We can realise all of the other gates by using just one single type of universal logic gate, the NAND (NOT AND) or the NOR (NOT OR) gate, thereby reducing the number of different types of logic gates required, and also the cost. Thus, the NAND and the NOR gates are commonly referred to as Universal Logic Gates. **Implementation of logic gates using NAND gate only:**



Implementation of logic gates using NOR gate only:



Boolean Algebra:

Boolean Algebra is used to analyse and simplify the digital (logic) circuits. It uses only the binary numbers i.e., 0 and 1. It is also called as Binary Algebra or logical Algebra. Boolean algebra was invented by George Boole in 1854.

Boolean Laws

There are six types of Boolean Laws.

Commutative law

Any binary operation which satisfies the following expression is referred to as commutative operation.

(i) $A.B = B.A$ (ii) $A + B = B + A$

Commutative law states that changing the sequence of the variables does not have any effect on the output of a logic circuit.

Associative law

This law states that the order in which the logic operations are performed is irrelevant as their effect is the same.

(i) $(A.B).C = A.(B.C)$ (ii) $(A + B) + C = A + (B + C)$

Distributive law

Distributive law states the following condition.

$A.(B + C) = A.B + A.C$

AND law

These laws use the AND operation. Therefore, they are called as **AND** laws.

(i) $A.0 = 0$ (ii) $A.1 = A$

(iii) $A.A = A$ (iv) $A.\overline{A} = 0$

OR law

These laws use the OR operation. Therefore, they are called as OR laws.

(i) $A + 0 = A$ (ii) $A + 1 = 1$

(iii) $A + A = A$ (iv) $A + \overline{A} = 1$

INVERSION law

This law uses the NOT operation. The inversion law states that double inversion of a variable results in the original variable itself.

$\overline{\overline{A}} = A$

Boolean Function:

Boolean algebra deals with binary variables and logic operation. A **Boolean Function** is described by an algebraic expression called **Boolean expression** which consists of binary variables, the constants 0 and 1, and the logic operation symbols. Consider the following example.

$F(A, B, C, D)$	=	$A + \overline{BC} + ADC$	Equation No. 1
Boolean Function		Boolean Expression	

Here the left side of the equation represents the output Y. So we can state equation no. 1

$Y = A + \overline{BC} + ADC$

Truth Table Formation

A truth table represents a table having all combinations of inputs and their corresponding result.

It is possible to convert the switching equation into a truth table. For example, consider the following switching equation.

$F(A, B, C) = A + BC$

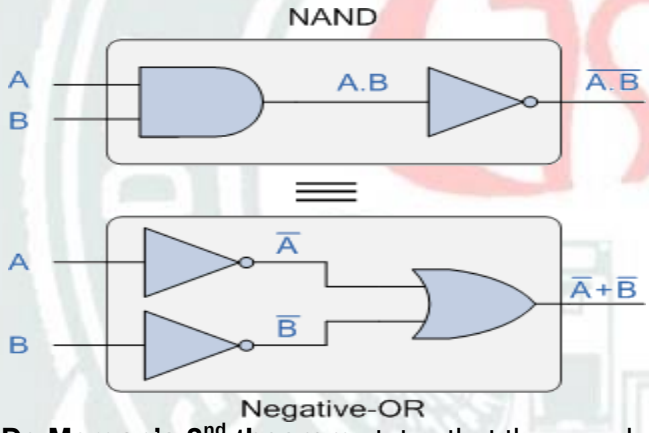
The output will be high (1) if A = 1 or BC = 1 or both are 1. The truth table for this equation is shown by Table (a). The number of rows in the truth table is 2^n where n is the number of input variables (n=3 for the given equation). Hence there are $2^3 = 8$ possible input combination of inputs.

Inputs			Output
A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

De Morgan's Theorem:

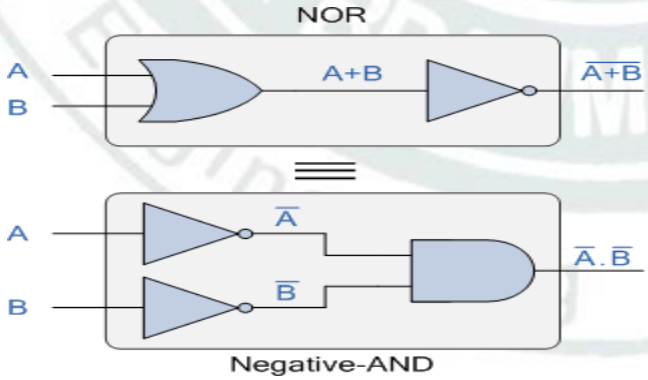
De Morgan's 1st theorem states that the complement of the product of all the terms is equal to the sum of the complement of each term.

$(A.B)' = A' + B'$



De Morgan's 2nd theorem states that the complement of the sum of all the terms is equal to the product of the complement of each term.

$(A + B)' = A'. B'$



Duality Theorem:

This theorem states that the dual of the Boolean function is obtained by interchanging the logical AND operator with logical OR operator and zeros with ones. For every Boolean function, there will be a corresponding Dual function.

Group1	Group2
x + 0 = x	x.1 = x
x + 1 = 1	x.0 = 0
x + x = x	x.x = x
x + x' = 1	x.x' = 0
x + y = y + x	x.y = y.x

Example-1:
Given Boolean function, f = p'qr + pq'r + pqr' + pqr.

Step 1 − Use the **Boolean postulate**, x + x = x. That means, the Logical OR operation with any Boolean variable 'n' times will be equal to the same variable. So, we can write the last term pqr two more times.

$$\Rightarrow f = p'qr + pq'r + pqr' + pqr + pqr + pqr$$

Step 2 − Use **Distributive law** for 1st and 4th terms, 2nd and 5th terms, 3rd and 6th terms.

$$\Rightarrow \quad f = qrp+pp+p + prq+qq+q + pqr+rr+r$$

Step 3 − Use **Boolean postulate**, x + x' = 1 for simplifying the terms present in eachparenthesis.

$$\Rightarrow f = qr11 + pr11 + pq11$$

Step 4 − Use **Boolean postulate**, x.1 = x for simplifying the above three terms.

$$\Rightarrow f = qr + pr + pq \Rightarrow f =$$

pq + qr + pr Therefore, the simplified Boolean function is **f =**

pq + qr + pr.

Example-2:
Let us find the complement **of the Boolean function, f = p'q + pq'.** The complement of Boolean function is f' = pq+pqpq+pq'.

Step 1 − Use DeMorgan's theorem, x+yx+y' = x'.y'. $\Rightarrow$ f'
= pqpq'.pqpq'

Step 2 − Use DeMorgan's theorem, x.yx.y' = x' + y'

$$\Rightarrow f' = \{pp' + q'\}.\{p' + qq'\}$$

Step3 - Use the Boolean postulate, $xx'=x$. $\Rightarrow f' = \{p + q'\}.\{p' + q\} \Rightarrow f' = pp' + pq + p'q' + qq'$

Step 4 – Use the Boolean postulate, $xx'=0$.

$$\Rightarrow f = 0 + pq + p'q' + 0 \Rightarrow$$

$$f = pq + p'q'$$

Therefore, the **complement** of Boolean function, p'q + pq' is **pq + p'q'**.

SOP and POS form:

Sum of Product (SOP):

- The Sum of Product expression is equivalent to the logical AND function which Sums two or more Products to produce an output.
- We will get four Boolean product terms by combining two variables x and y with logical AND operation.
- These Boolean product terms are called as **min terms** or **standard product terms**.
  - If the binary variable is '0', then it is represented as complement of variable and '1' as normal form in min term. The min terms are x'y', x'y, xy' and xy. **Product of Sum (POS):**
- The Product of Sum expression is equivalent to the logical OR-AND function which gives the AND Product of two or more OR Sums to produce an output.
- We will get four Boolean sum terms by combining two variables x and y with logical OR operation.
- These Boolean sum terms are called as **Max terms** or **standard sum terms**. If the binary variable is '1', then it is represented as complement of variable and '0' as normal form in Max term. The Max terms are x + y, x + y', x' + y and x' + y'.

x	y	Min terms	Max terms
0	0	$m_0=x'y'$	$M_0=x + y$
0	1	$m_1=x'y$	$M_1=x + y'$
1	0	$m_2=xy'$	$M_2=x' + y$
1	1	$m_3=xy$	$M_3=x' + y'$

Canonical SOP and POS forms:

- A truth table consists of a set of inputs and outputs.
- If there are 'n' input variables, then there will be 2^n possible combinations with zeros and ones.

- So, the value of each output variable depends on the combination of input variables.
  - So, each output variable will have '1' for some combination of input variables and '0' for some other combination of input variables.

Therefore, we can express each output variable in following two ways.

- Canonical SOP form
- Canonical POS form

Canonical SOP form:

- Canonical SOP form means Canonical Sum of Products form.
- In this form, each product term contains all literals.
- So, these product terms are nothing but the min terms. Hence, canonical SOP form is also called as **sum of min terms** form.
- First, identify the min terms for which, the output variable is one and then do the logical OR of those min terms in order to get the Boolean expression function corresponding to that output variable. This Boolean function will be in the form of sum of min terms.
- Follow the same procedure for other output variables also, if there is more than one output variable. **Example**

Consider the following **truth table**.

Inputs			Ou put
p	**Q**	**r**	**f**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

- Here, the output f is '1' for four combinations of inputs.
- The corresponding min terms are p'qr, pq'r, pqr', pqr.
- By doing logical OR of these four min terms, we will get the Boolean function of output f.

Therefore, the Boolean function of output is, f
= p'qr + pq'r + pqr' + pqr.
This is the **canonical SOP form** of output, f. We can also represent this function in following two notations.

$$f = m3+m5+m6+m7 \quad f=\sum m(3,5,6,7)$$

In one equation, we represented the function as sum of respective min terms. In other equation, we used the symbol for summation of those min terms.

Canonical POS form:

- Canonical POS form means Canonical Product of Sums form.

- In this form, each sum term contains all literals. So, these sum terms are nothing but the Max terms. Hence, canonical POS form is also called as **product of Max terms** form.
- First, identify the Max terms for which, the output variable is zero and then do the logical AND of those Max terms in order to get the Boolean expression function corresponding to that output variable. This Boolean function will be in the form of product of Max terms.
- Follow the same procedure for other output variables also, if there is more than one output variable.

Example

- Consider the same truth table of previous example.
- Here, the output f is '0' for four combinations of inputs.
- The corresponding Max terms are p + q + r, p + q + r', p + q' + r, p' + q + r.
- By doing logical AND of these four Max terms, we will get the Boolean function of output f.

Therefore, the Boolean function of output is, f
= (p+q+r). (p+q+r). (p+q+r). (p+q+r).
This is the **canonical POS form** of output, f.
We can also represent this function in following two notations. f=M0.M1.M2.M4

$$f=\prod M(0,1,2,4)$$

In one equation, we represented the function as product of respective Max terms. In other equation, we used the symbol for multiplication of those Max terms. The Boolean function,
f = (p+q+r). (p+q+r). (p+q+r). (p+q+r)
is the dual of the Boolean function, f
= p'qr + pq'r + pqr' + pqr.
Therefore, both canonical SOP and canonical POS forms are **Dual** to each other. Functionally, these two forms are same. Based on the requirement, we can use one of these two forms.

Standard SOP and POS forms

We discussed two canonical forms of representing the Boolean outputs. Similarly, there are two standard forms of representing the Boolean outputs. These are the simplified version of canonical forms.

- Standard SOP form
- Standard POS form

The main **advantage** of standard forms is that the number of inputs applied to logic gates can be minimized. Sometimes, there will be reduction in the total number of logic gates required.

Standard SOP form:

Standard SOP form means **Standard Sum of Products** form. In this form, each product term need not contain all literals. So, the product terms may or may not be the min terms.
Therefore, the Standard SOP form is the simplified form of canonical SOP form.
We will get Standard SOP form of output variable in two steps.

- Get the canonical SOP form of output variable
- Simplify the above Boolean function, which is in canonical SOP form.

Follow the same procedure for other output variables also, if there is more than one output variable. Sometimes, it may not possible to simplify the canonical SOP form. In that case, both canonical and standard SOP forms are same.

Example

Convert the following Boolean function into Standard SOP form. f
= p'qr + pq'r + pqr' + pqr
The given Boolean function is in canonical SOP form. Now, we have to simplify this Boolean function in order to get standard SOP form.

Step 1 − Use the **Boolean postulate**, x + x = x. That means, the Logical OR operation with any Boolean variable 'n' times will be equal to the same variable. So, we can write the last term pqr two more times.

$$\Rightarrow f = p'qr + pq'r + pqr' + pqr + pqr + pqr$$

Step 2 − Use **Distributive law** for 1st and 4th terms, 2nd and 5th terms, 3rd and 6th terms.f ⇒

$$= qr\,(p+p) + pr\,(q+q) + pq\,(r+r)$$

Step 3 − Use **Boolean postulate**, x + x' = 1 for simplifying the terms present in each parenthesis. ⇒= qr 1 + pr 1 + pq 1

Step 4 − Use **Boolean postulate**, x.1 = x for simplifying above three terms.

$$\Rightarrow f = qr + pr + pq \Rightarrow$$

$$f = pq + qr + pr$$

This is the simplified Boolean function. Therefore, the **standardSOP form** corresponding to given canonical SOP form is **f = pq + qr + prStandard POS form:**

Standard POS form means **Standard Product of Sums** form. In this form, each sum term need not contain all literals. So, the sum terms may or may not be the Max terms. Therefore, the Standard POS form is the simplified form of canonical POS form.

We will get Standard POS form of output variable in two steps.

- Get the canonical POS form of output variable
- Simplify the above Boolean function, which is in canonical POS form.

Follow the same procedure for other output variables also, if there is more than one output variable. Sometimes, it may not possible to simplify the canonical POS form. In that case, both canonical and standard POS forms are same.

Example

Convert the following Boolean function into Standard POS form.

$$f = (p+q+r).\,(p+q+r).\,(p+q+r).\,(p+q+r)$$

The given Boolean function is in canonical POS form. Now, we have to simplify this Boolean function in order to get standard POS form.

Step 1 − Use the **Boolean postulate**, x.x = x. That means, the Logical AND operation with any Boolean variable 'n' times will be equal to the same variable. So, we can write the first term p+q+r two more times.

$$\Rightarrow f = (p+q+r).\,(p+q+r).\,(p+q+r).\,(p+q+r).\,(p+q+r).\,(p+q+r)$$

Step 2 − Use **Distributive law,** x + y.z = (x+y). (x+z) for 1st and 4th parenthesis, 2nd and 5th parenthesis, 3rd and 6th parenthesis.

$$\Rightarrow f = (p+q+rr).\,(p+r+qq).\,(q+r+pp)$$

Step 3 − Use **Boolean postulate**, x.x'=0 for simplifying the terms present in each parenthesis. f

$$\Rightarrow = (p+q+0).\,(p+r+0).\,(q+r+0)$$

Step 4 − Use **Boolean postulate**, x + 0 = x for simplifying the terms present in each parenthesis ⇒= (p+q). (p+r). (q+r) f ⇒(p+q). (q+r). (p+r)

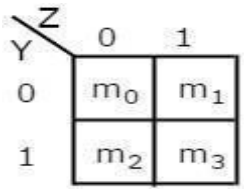
This is the simplified Boolean function. Therefore, the **standard POS form** corresponding to given canonical POS form is **f = (**p+q**). (**q+r**). (**p+r). This is the **dual** of the Boolean function, f = pq + qr + pr.

Therefore, both Standard SOP and Standard POS forms are Dual to each other. **Karnaugh map:**

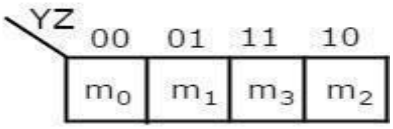
- Karnaugh introduced a method for simplification of Boolean functions in an easy way. This method is known as Karnaugh map method or K-map method.
- It is a graphical method, which consists of 2n cells for 'n' variables. The adjacent cells are differed only in single bit position.

2- Variable K-Map:

The number of cells in 2 variable K-map is four, since the number of variables is two.



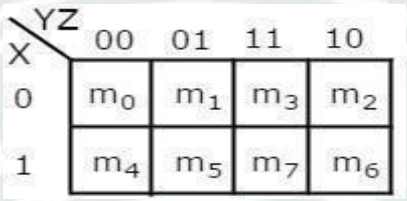
or



- There is only one possibility of grouping 4 adjacent min terms.
- The possible combinations of grouping 2 adjacent min terms are {(m_0, m_1), (m_2, m_3), (m_0, m_2) and (m_1, m_3)}. **3-Variable**

K-Map:

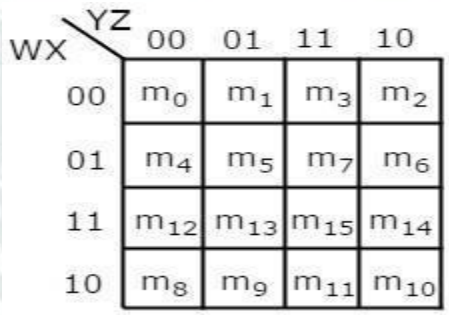
The number of cells in 3 variable K-map is eight, since the number of variables is three.

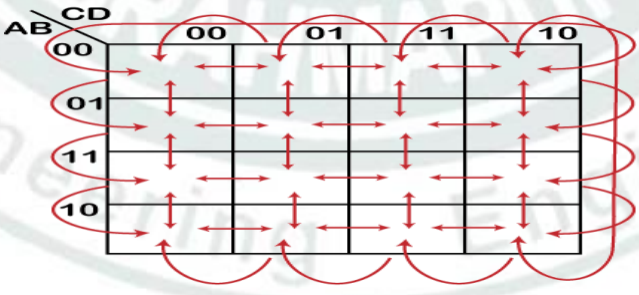


- There is only one possibility of grouping 8 adjacent min terms.
- The possible combinations of grouping 4 adjacent min terms are {(m_0, m_1, m_3, m_2), (m_4, m_5, m_7, m_6), (m_0, m_1, m_4, m_5), (m_1, m_3, m_5, m_7), (m_3, m_2, m_7, m_6) and (m_2, m_0, m_6, m_4)}.
- The possible combinations of grouping 2 adjacent min terms are {(m_0, m_1), (m_1, m_3), (m_3, m_2), (m_2, m_0), (m_4, m_5), (m_5, m_7), (m_7, m_6), (m_6, m_4), (m_0, m_4), (m_1, m_5), (m_3, m_7) and (m_2, m_6)}.
- If x=0, then 3 variable K-map becomes 2 variable K-map.

4- Variable K-Map:

The number of cells in 4 variable K-map is sixteen, since the number of variables is four.



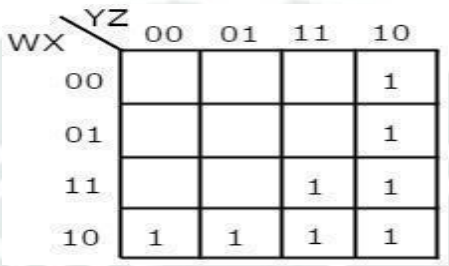


- There is only one possibility of grouping 16 adjacent min terms.
- Let R_1, R_2, R_3 and R_4 represents the min terms of first row, second row, third row and fourth row respectively. Similarly, C_1, C_2, C_3 and C_4 represents the min terms of first column, second column, third column and fourth column respectively. The possible

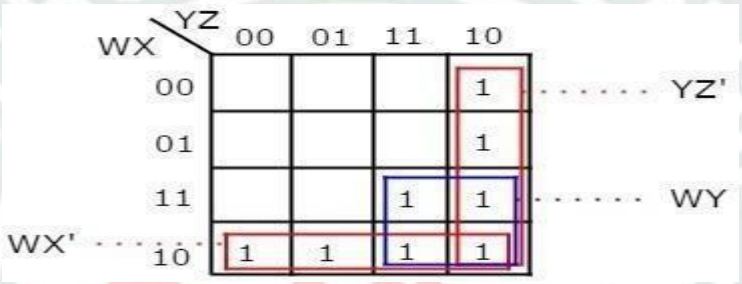
combinations of grouping 8 adjacent min terms are {(R_1, R_2), (R_2, R_3), (R_3, R_4), (R_4, R_1), (C_1, C_2), (C_2, C_3), (C_3, C_4), (C_4, C_1)}.

- If w=0, then 4 variable K-map becomes 3 variable K-map.

Example- **f(**W,X,Y,Z)**= ∑m(2,6,8,9,10,11,14,15)**
using K-map.
The given Boolean function is in sum of products form. It is having 4 variables W, X, Y & Z.
So, we require **4 variable K-map**.

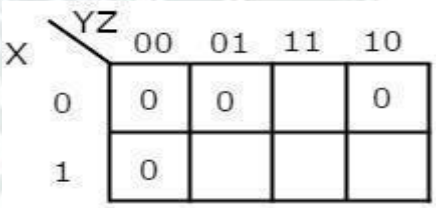


The **4 variable K-map** with three **groupings** is

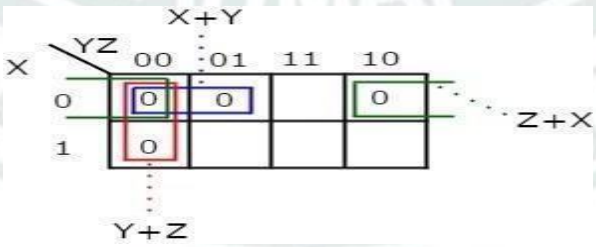


Therefore, the **simplified Boolean function** is **f = WX' + WY + YZ'**

Example- f(X,Y,Z)=∏M(0,1,2,4)
using K-map.
The given Boolean function is in product of Max terms form. It is having 3 variables X, Y & Z.
So, we require 3 variable K-map.



The **3 variable K-map** with three **groupings** is



Therefore, the **simplified Boolean function** is

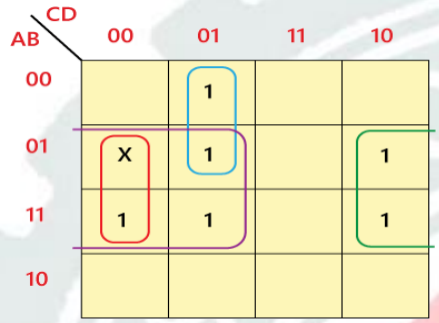
f = (X+Y**). (**Y+Z**). (**Z+X)

Don't care condition:

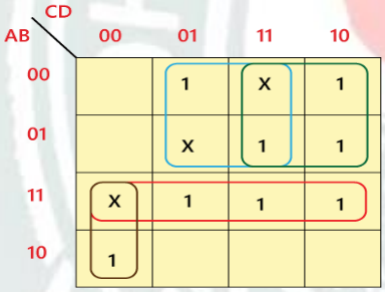
- The "Don't care" condition says that we can use the blank cells of a K-map to make a group of the variables.

- To make a group of cells, we can use the "don't care" cells as either 0 or 1, and if required, we can also ignore that cell.
- We mainly use the "don't care" cell to make a large group of cells.
- The cross(X) symbol is used to represent the "don't care" cell in K-map.
- This cross symbol represents an invalid combination.
- The "don't care" in excess-3 code are 0000, 0001, 0010, 1101, 1110, and 1111 because they are invalid combinations.
- Apart from this, the 4-bit BCD to Excess-3 code, the "don't care" are 1010, 1011, 1100, 1101, 1110, and 1111.

Example 1: Minimize f = ∑m(1,5,6,12,13,14) + d(4) in SOP minimal form



So, the minimized SOP form of the function is:
f = BC' + BD' + A'C'D **Example-2:**
Minimize the following function in SOP minimal form using K-Maps: F(A, B, C, D) = ∑m(1, 2, 6, 7, 8, 13, 14, 15) + d(3, 5, 12)



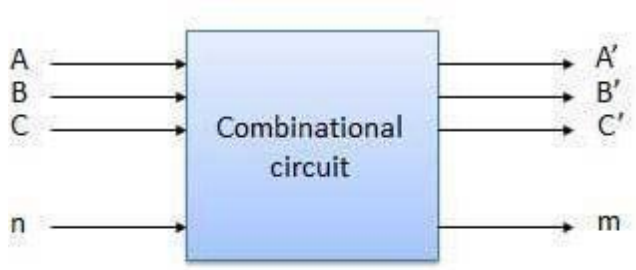
F = AC'D' + A'D + A'C + AB

UNIT-2Combinational logic circuit

Combinational circuit is a circuit in which we combine the different gates in the circuit, for example encoder, decoder, multiplexer and demultiplexer. Some of the characteristics of combinational circuits are following −

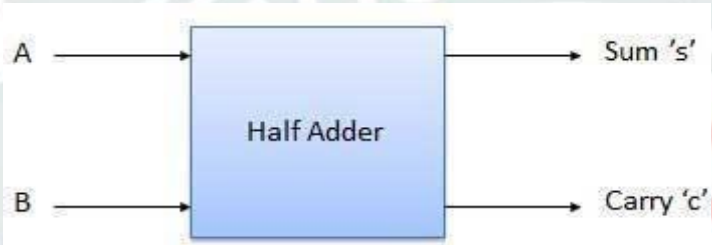
- The output of combinational circuit at any instant of time, depends only on the levels present at input terminals.
- The combinational circuit do not use any memory. The previous state of input does not have any effect on the present state of the circuit.
- A combinational circuit can have an n number of inputs and m number of outputs.

Block Diagram:



Half Adder

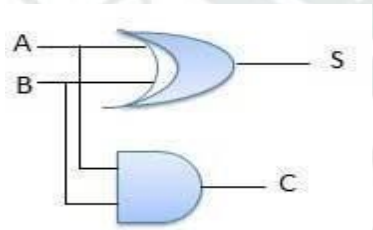
Half adder is a combinational logic circuit with two inputs and two outputs. The half adder circuit is designed to add two single bit binary number A and B. It is the basic building block for addition of two **single** bit numbers. This circuit has two outputs **carry** and **sum**. Block diagram



Truth Table

Inputs		Output	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

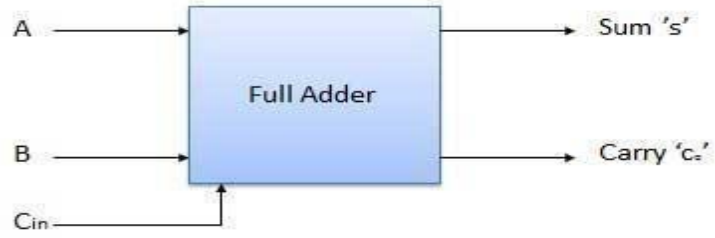
Circuit Diagram



Full Adder

Full adder is developed to overcome the drawback of Half Adder circuit. It can add two onebit numbers A and B, and carry c. The full adder is a three input and two output combinational circuit.

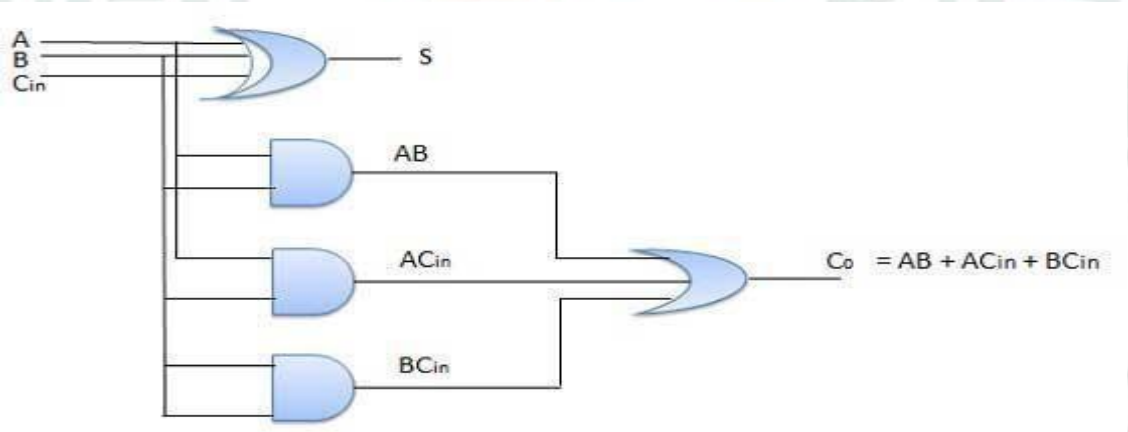
Block diagram



Truth Table

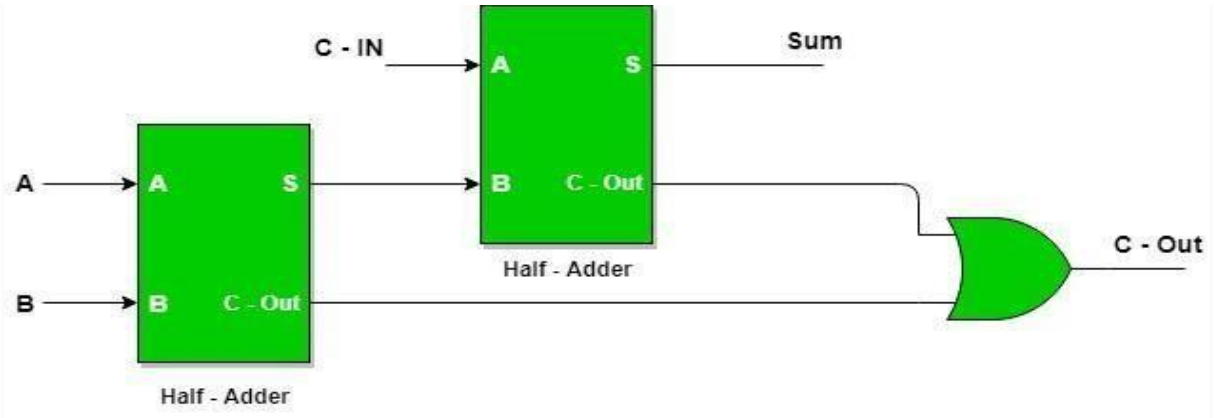
Inputs			Output	
A	B	Cin	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Circuit Diagram



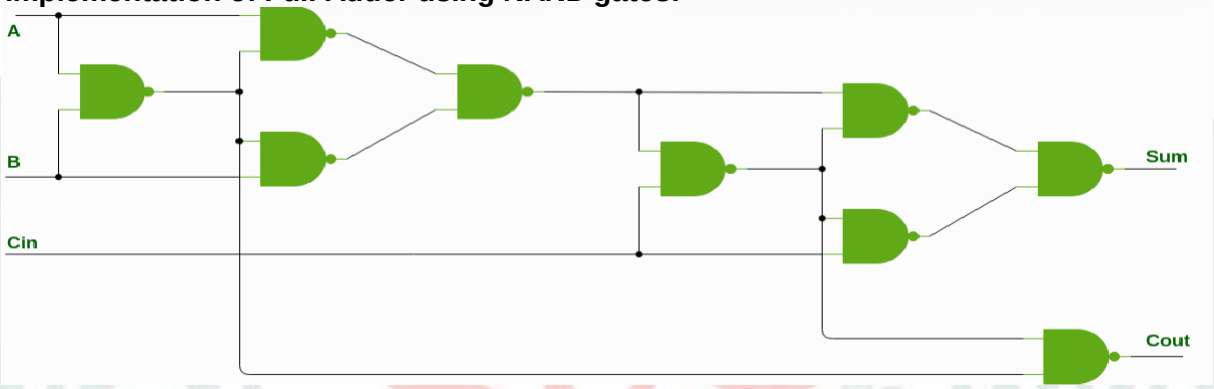
Implementation of Full Adder using Half Adders

2 Half Adders and a OR gate is required to implement a Full Adder.



With this logic circuit, two bits can be added together, taking a carry from the next lower order of magnitude, and sending a carry to the next higher order of magnitude.

Implementation of Full Adder using NAND gates:

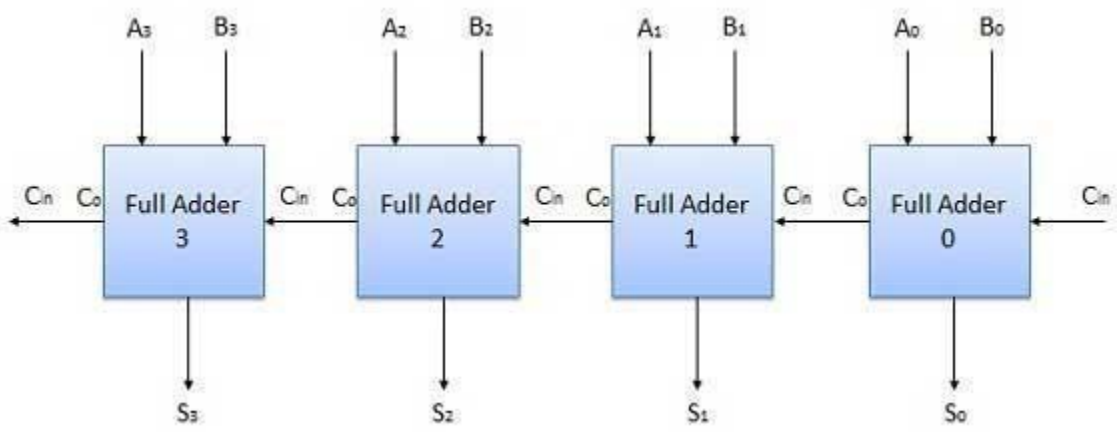


The Full Adder is capable of adding only two single digit binary number along with a carry input. But in practical we need to add binary numbers which are much longer than just one bit. To add two n-bit binary numbers we need to use the n-bit parallel adder. It uses a number of full adders in cascade. The carry output of the previous full adder is connected to carry input of the next full adder.

4 Bit Parallel Adder

In the block diagram, A_0 and B_0 represent the LSB of the four bit words A and B. Hence Full Adder-0 is the lowest stage. Hence its C_{in} has been permanently made 0. The rest of the connections are exactly same as those of n-bit parallel adder is shown in fig. The four-bit parallel adder is a very common logic circuit.

Block diagram



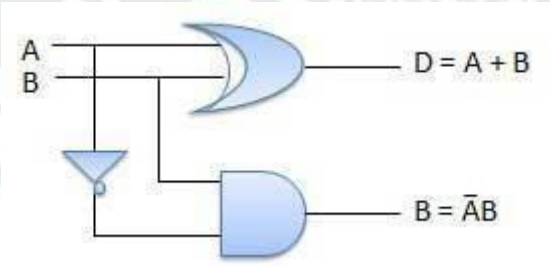
Half Subtractors

Half subtractor is a combination circuit with two inputs and two outputs (difference and borrow). It produces the difference between the two binary bits at the input and also produces an output (Borrow) to indicate if a 1 has been borrowed. In the subtraction (A-B), A is called as Minuend bit and B is called as Subtrahend bit.

Truth Table

Inputs		Output	
A	B	(A – B)	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Circuit Diagram



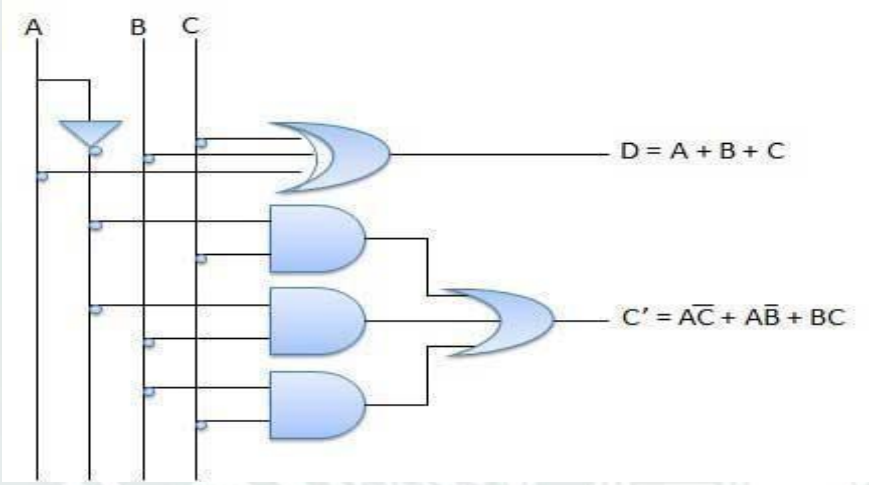
Full Subtractors

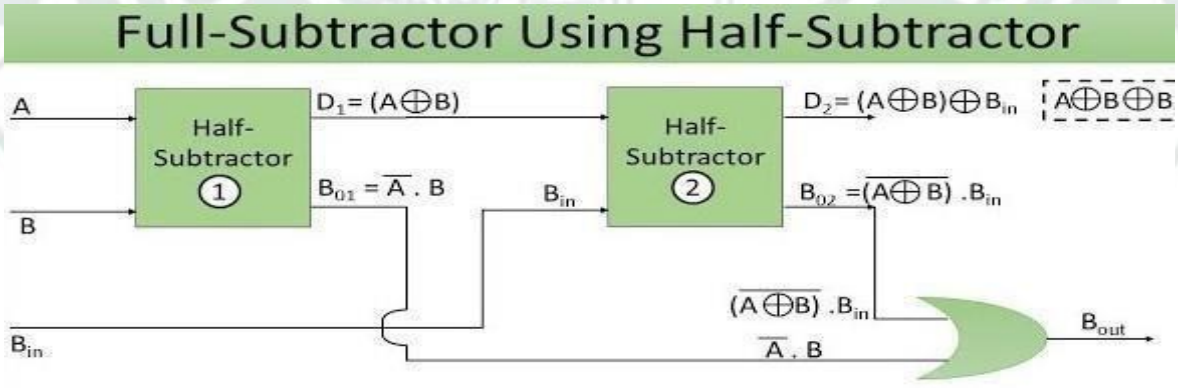
The disadvantage of a half subtractor is overcome by full subtractor. The full subtractor is a combinational circuit with three inputs A,B,C and two output D and C'. A is the 'minuend', B is 'subtrahend', C is the 'borrow' produced by the previous stage, D is the difference output and C' is the borrow output.

Truth Table

Inputs			Output	
A	B	C	(A-B-C)	C'
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Circuit Diagram



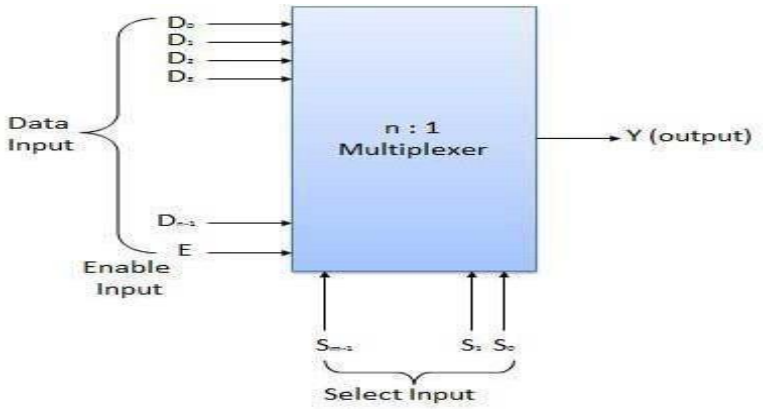


Multiplexers

Multiplexer is a special type of combinational circuit. There are n-data inputs, one output and m select inputs with 2m = n. It is a digital circuit which selects one of the n data inputs and routes it to the output. The selection of one of the n inputs is done by the selected inputs. Depending on the digital code applied at the selected inputs, one out of n data sources is selected and transmitted to the single output Y. E is called the strobe or enable input which is

useful for the cascading. It is generally an active low terminal that means it will perform the required operation when it is low.

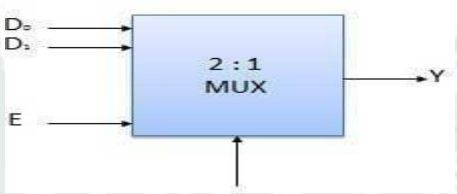
Block diagram



Multiplexers come in multiple variations

- 2 : 1 multiplexer
- 4 : 1 multiplexer
- 16 : 1 multiplexer
- 32 : 1 multiplexer

Block Diagram



Truth Table

Enable	Select	Output
E	S	Y
0	x	0
1	0	D_0
1	1	D_1

x = Don't care

Demultiplexers

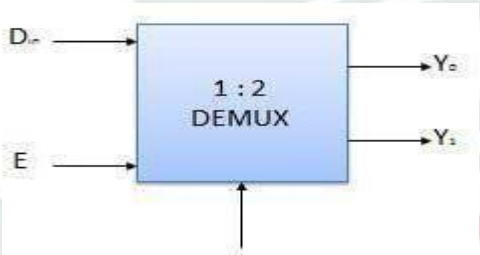
A demultiplexer performs the reverse operation of a multiplexer i.e. it receives one input and distributes it over several outputs. It has only one input, n outputs, m select input. At a time

only one output line is selected by the select lines and the input is transmitted to the selected output line. A de-multiplexer is equivalent to a single pole multiple way switch as shown in fig.

Demultiplexers comes in multiple variations.

- 1 : 2 demultiplexer
- 1 : 4 demultiplexer
- 1 : 16 demultiplexer
- 1 : 32 demultiplexer

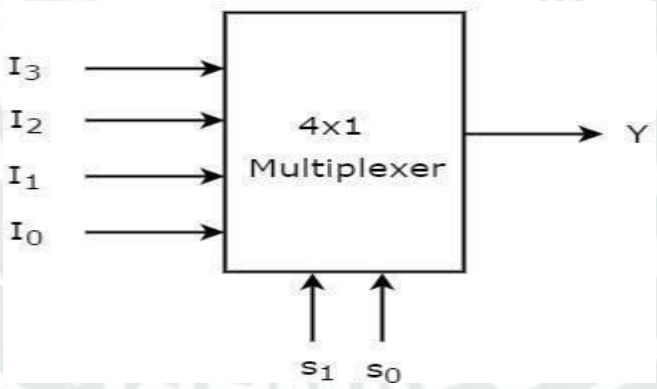
Block diagram



Truth Table

4:1 Multiplexer

4:1 Multiplexer has four data inputs I_3, I_2, I_1& I_0, two selection lines s_1& s_0 and one output Y. The **block diagram** of 4x1 Multiplexer is shown in the following figure.



One of these 4 inputs will be connected to the output based on the combination of inputs present at these two selection lines.

Truth table of 4:1 Multiplexer is shown below.

Selection Lines		Output
S_1	**S_0**	**Y**
0	0	I_0

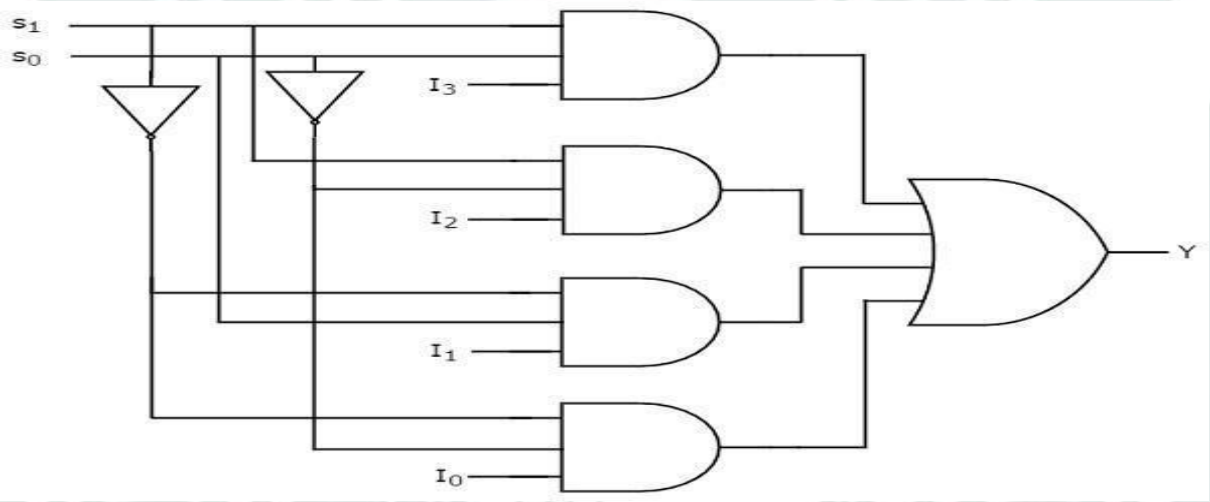
0	1	I_1
1	0	I_2
1	1	I_3

From Truth table, we can directly write the **Boolean function** for output, Y as

$$Y = S1'S0'I_0 + S1'S0I_1 + S1S0'I_2 + S1S0I_3$$

We can implement this Boolean function using Inverters, AND gates & OR gate.

The **circuit diagram** of 4:1 multiplexer is shown in the following figure.



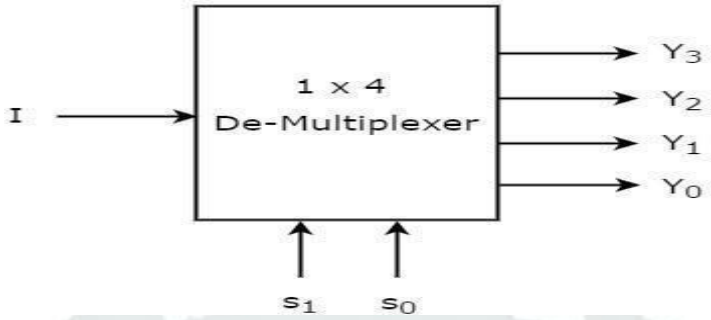
We can easily understand the operation of the above circuit. Similarly, you can implement 8x1 Multiplexer and 16x1 multiplexer by following the same procedure.

Enable	Select	Output	
E	S	Y0	Y1
0	x	0	0
1	0	0	D_{in}
1	1	D_{in}	0

x = Don't care

1:4 De-Multiplexer

1:4 De-Multiplexer has one input I, two selection lines, s_1& s_0 and four outputs Y_3, Y_2, Y_1&Y_0. The **block diagram** of 1:4 De-Multiplexer is shown in the following figure.



The single input 'I' will be connected to one of the four outputs, Y_3 to Y_0 based on the values of selection lines s_1& s0. The **Truth table** of 1x4 De-Multiplexer is shown below.

Selection Inputs		**Outputs**			
S_1	**S_0**	**Y_3**	**Y_2**	**Y_1**	**Y_0**
0	0	0	0	0	**I**
0	1	0	0	**I**	0
1	0	0	**I**	0	0
1	1	**I**	0	0	0

From the above Truth table, we can directly write the **Boolean functions** for each output as

$$Y3 = s_1 s_0 I$$

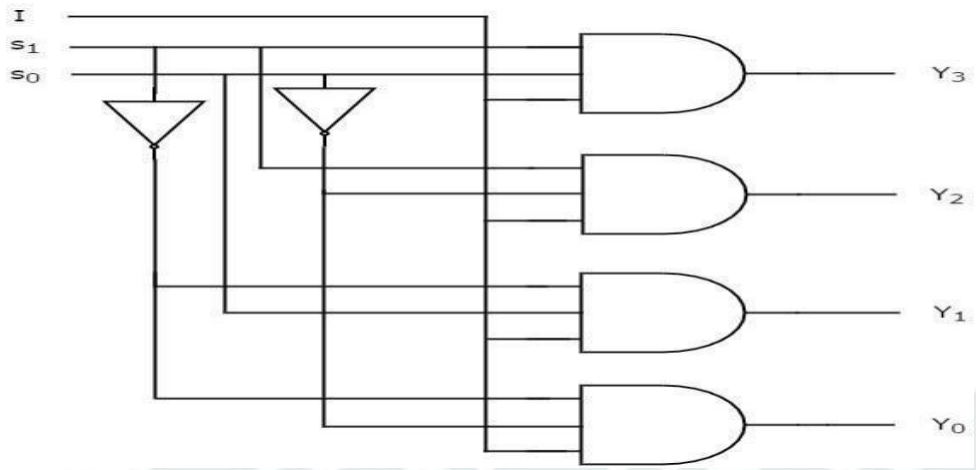
$$Y2 = s1 s0' I$$

$$Y1 = s1' s0 I$$

$$Y0 = s1' s0' I$$

We can implement these Boolean functions using Inverters & 3-input AND gates.

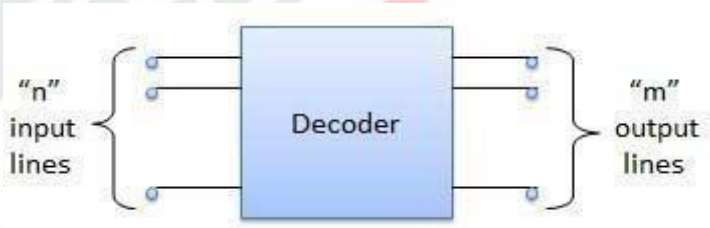
The **circuit diagram** of 1:4 De-Multiplexer is shown in the following figure.



Decoder

A decoder is a combinational circuit. It has n input and to a maximum m = 2n outputs. Decoder is identical to a demultiplexer without any data input. It performs operations which are exactly opposite to those of an encoder.

Block diagram



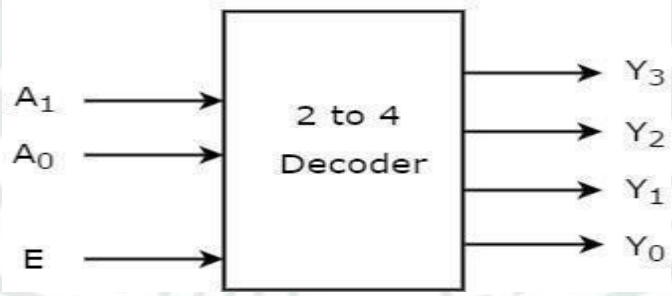
Examples of Decoders are following.

- Code converters
- BCD to seven segment decoders

2 to 4 Decoder

Let 2 to 4 Decoder has two inputs A_1& A_0 and four outputs Y_3, Y_2, Y_1& Y_0.

The **block diagram** of 2 to 4 decoder is shown in the following figure.



One of these four outputs will be '1' for each combination of inputs when enable, E is '1'.

The **Truth table** of 2 to 4 decoder is shown below.

Enable	Inputs	Outputs

E	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

From Truth table, we can write the **Boolean functions** for each output as

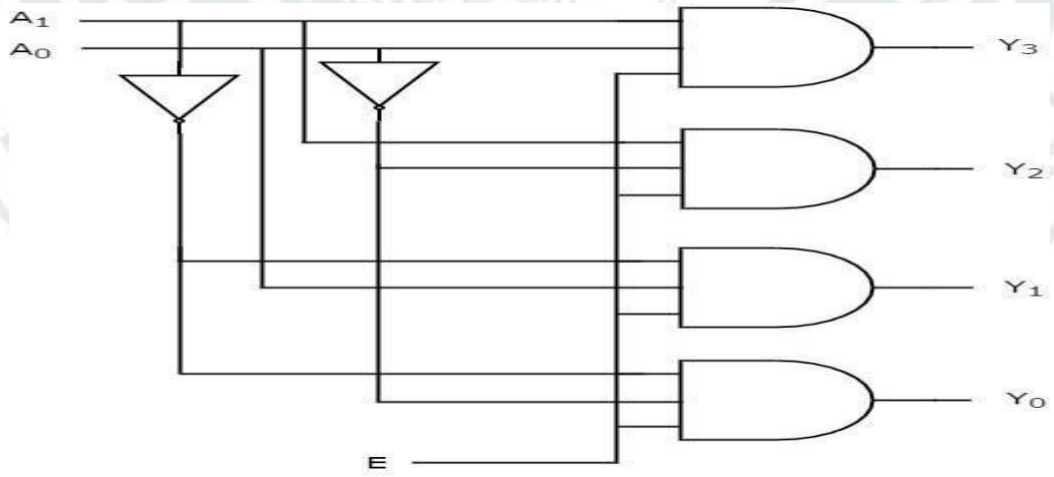
$$Y3 = E.A1.A0$$

$$Y2 = E.A1.A0'$$

$$Y1 = E.A1'.A0$$

$$Y0 = E.A1'.A0'$$

Each output is having one product term. So, there are four product terms in total. We can implement these four product terms by using four AND gates having three inputs each & two inverters. The **circuit diagram** of 2 to 4 decoder is shown in the following figure.

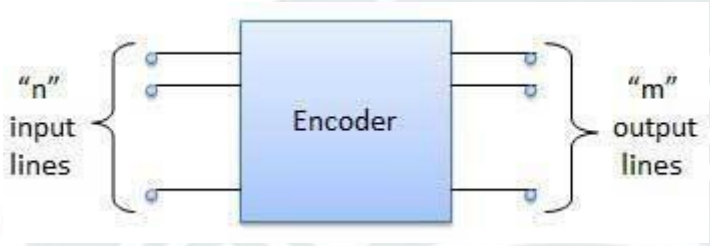


Therefore, the outputs of 2 to 4 decoder are nothing but the **min terms** of two input variables A_1& A_0, when enable, E is equal to one. If enable, E is zero, then all the outputs of decoder will be equal to zero.

Similarly, 3 to 8 decoder produces eight min terms of three input variables A_2, A_1& A_0 and 4 to 16 decoder produces sixteen min terms of four input variables A_3, A_2, A_1& A_0.

Encoder

Encoder is a combinational circuit which is designed to perform the inverse operation of the decoder. An encoder has n number of input lines and m number of output lines. An encoder produces an m bit binary code corresponding to the digital input number. The encoder accepts an n input digital word and converts it into an m bit another digital word. Block diagram



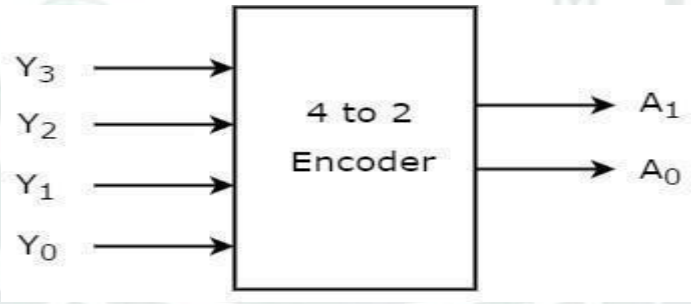
Examples of Encoders are following.

- Priority encoders
- Decimal to BCD encoder
- Octal to binary encoder
- Hexadecimal to binary encoder

4 to 2 Encoder

Let 4 to 2 Encoder has four inputs Y_3, Y_2, Y_1& Y_0 and two outputs A_1& A_0.

The **block diagram** of 4 to 2 Encoder is shown in the following figure.



At any time, only one of these 4 inputs can be '1' in order to get the respective binary code at the output. The **Truth table** of 4 to 2 encoder is shown below.

Inputs				**Outputs**	
Y_3	**Y_2**	**Y_1**	**Y_0**	**A_1**	**A_0**
0	0	0	1	0	0

0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

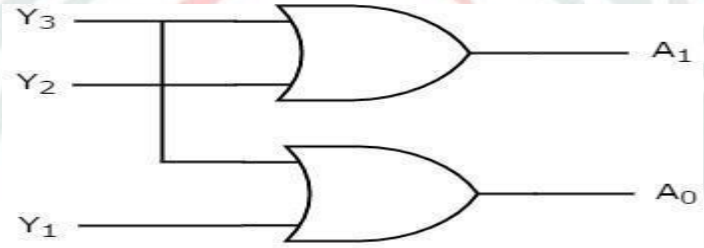
From Truth table, we can write the **Boolean functions** for each output as

$$A1 = Y3 + Y2$$

$$A0 = Y3 + Y1$$

We can implement the above two Boolean functions by using two input OR gates.

The **circuit diagram** of 4 to 2 encoder is shown in the following figure.

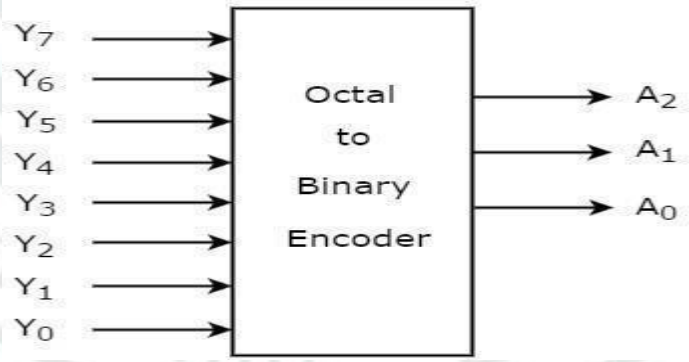


The above circuit diagram contains two OR gates. These OR gates encode the four inputs with two bits

Octal to Binary Encoder

Octal to binary Encoder has eight inputs, Y_7 to Y_0 and three outputs A_2, A_1& A_0. Octal to binary encoder is nothing but 8 to 3 encoder.

The **block diagram** of octal to binary Encoder is shown in the following figure.



At any time, only one of these eight inputs can be '1' in order to get the respective binary code.
The **Truth table** of octal to binary encoder is shown below.

Inputs	Outputs

Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

From Truth table, we can write the **Boolean functions** for each output as

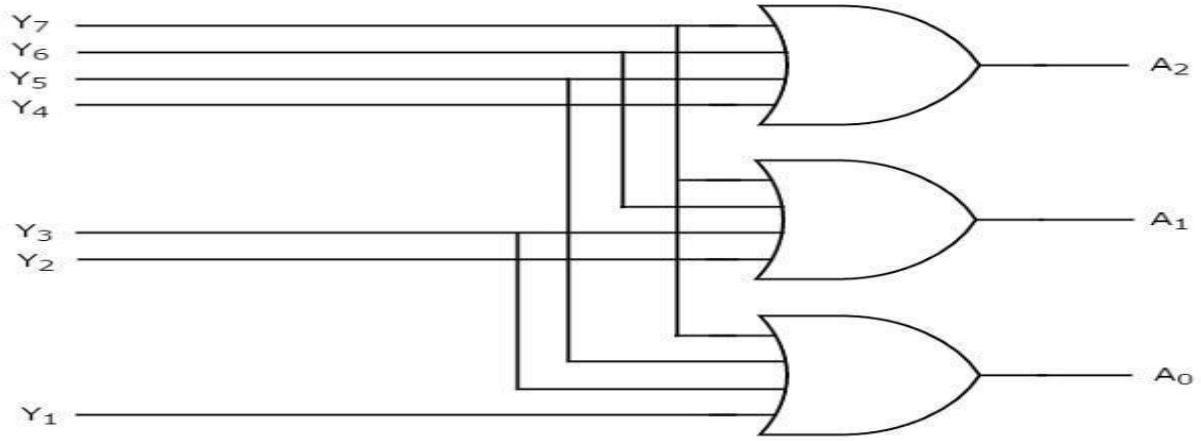
$$A2 = Y7 + Y6 + Y5 + Y4$$

$$A1 = Y7 + Y6 + Y3 + Y2$$

$$A0 = Y7 + Y5 + Y3 + Y1$$

We can implement the above Boolean functions by using four input OR gates.

The **circuit diagram** of octal to binary encoder is shown in the following figure.

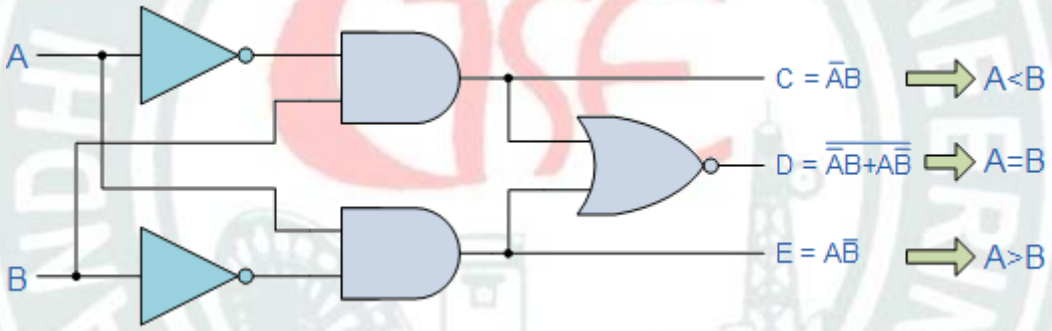


The above circuit diagram contains three 4-input OR gates. These OR gates encode the eight inputs with three bits.

Digital comparator

The Digital Comparator is another very useful combinational logic circuit used to compare the value of two binary digits.

1- bit Digital Comparator Circuit



Then the operation of a 1-bit digital comparator is given in the following Truth Table. **Digital Comparator Truth Table**

Inputs		Outputs		
B	A	A > B	A = B	A < B
0	0	0	1	0

0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

2- bit Magnitude Comparator

A comparator that compares two binary numbers (each number having 2 bits) and produces three outputs based on the relative magnitudes of given binary bits is called a 2-bit magnitude comparator.

Truth Table

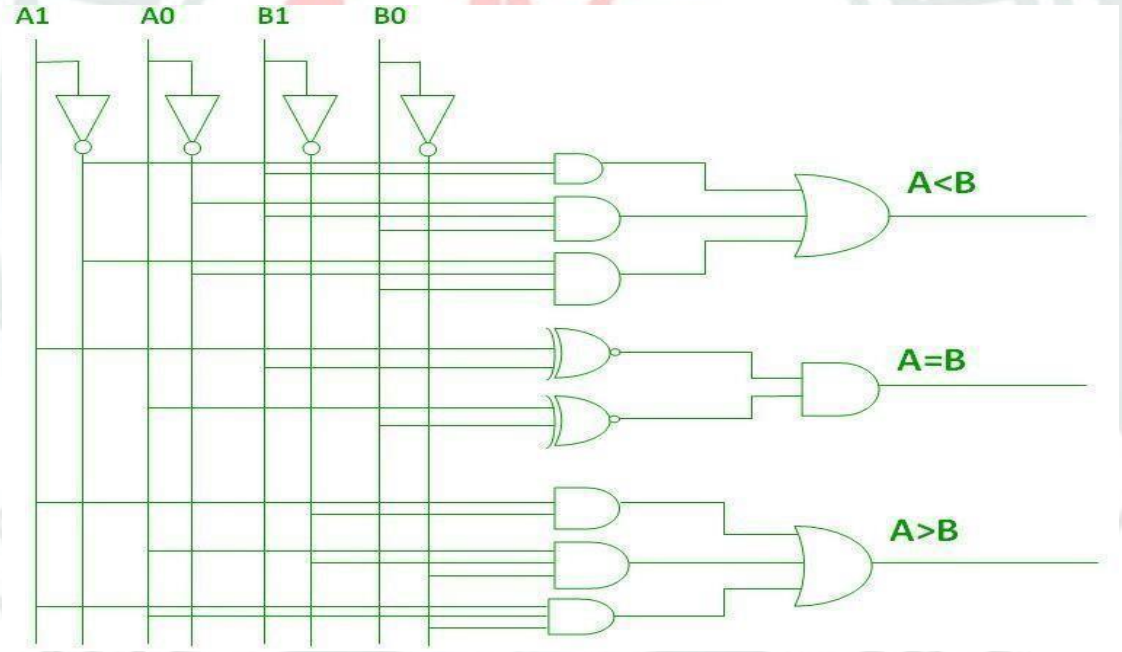
A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1

1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

The truth table derives the expressions of A<B, A>B, and A=B as below

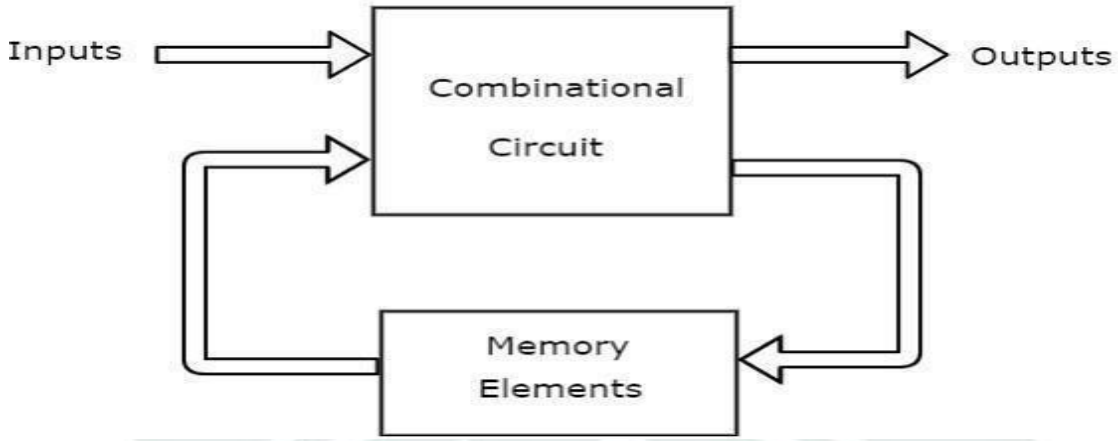
$$A < B - A1'B1' + A0'B1B0 + A1'A0'B0$$
$$A > B - A1B1' + A0B1'B0' + A1A0B0'$$
$$A = B - (A0\ Ex-Nor\ B0)\ (A1\ Ex-Nor\ B1)$$

With these expressions, the Circuit diagram can be as follows



UNIT-3
Sequential Logic Circuits

Sequential circuit contains a set of inputs and outputs. The outputs of sequential circuit depend not only on the combination of present inputs but also on the previous outputs. Previous output is nothing but the **present state**. Therefore, sequential circuits contain combinational circuits along with memory storage elements. Some sequential circuits may not contain combinational circuits, but only memory elements.



Following table shows the **differences** between combinational circuits and sequential circuits.

Combinational Circuits	Sequential Circuits
Outputs depend only on present inputs.	Outputs depend on both present inputs and present state.
Feedback path is not present.	Feedback path is present.
Memory elements are not required.	Memory elements are required.
Clock signal is not required.	Clock signal is required.
Easy to design.	Difficult to design.

Types of Sequential Circuits

Following are the two types of sequential circuits −

- Asynchronous sequential circuits
- Synchronous sequential circuits

Asynchronous sequential circuits

If some or all the outputs of a sequential circuit do not change affect with respect to active transition of clock signal, then that sequential circuit is called as **Asynchronous sequential circuit**. That means, all the outputs of asynchronous sequential circuits do not change affect at the same time. Therefore, most of the outputs of asynchronous sequential circuits are **not in synchronous** with either only positive edges or only negative edges of clock signal.

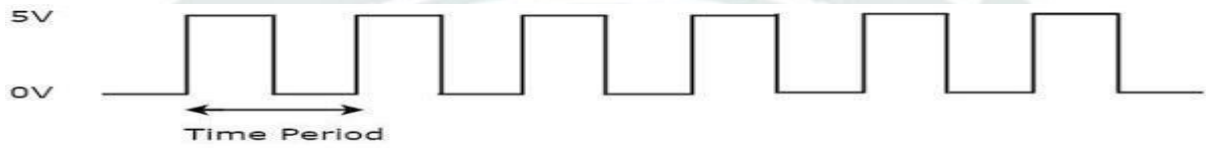
Synchronous sequential circuits

If all the outputs of a sequential circuit change affect with respect to active transition of clock signal, then that sequential circuit is called as **Synchronous sequential circuit**. That means, all the outputs of synchronous sequential circuits change affect at the same time. Therefore, the outputs of synchronous sequential circuits are in synchronous with either only positive edges or only negative edges of clock signal.

Clock Signal and Triggering

Clock signal

Clock signal is a periodic signal and its ON time and OFF time need not be the same. We can represent the clock signal as a **square wave**, when both its ON time and OFF time are same. This clock signal is shown in the following figure.



Types of Triggering

Following are the two possible types of triggering that are used in sequential circuits.

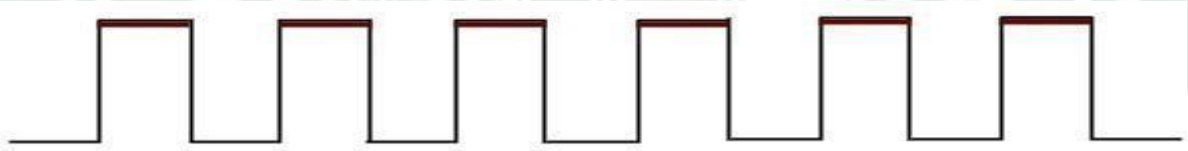
- Level triggering
- Edge triggering

Level triggering

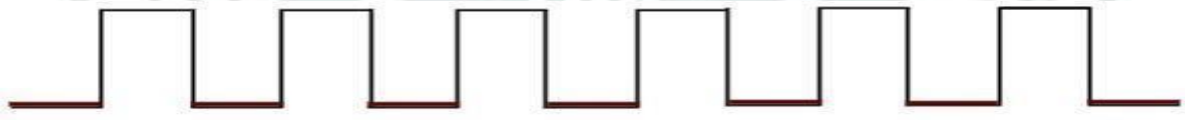
There are two levels, namely logic High and logic Low in clock signal. Following are the two **types of level triggering**.

- Positive level triggering
- Negative level triggering

If the sequential circuit is operated with the clock signal when it is in **Logic High**, then that type of triggering is known as **Positive level triggering**. It is highlighted in below figure.



If the sequential circuit is operated with the clock signal when it is in **Logic Low**, then that type of triggering is known as **Negative level triggering**. It is highlighted in the following figure.



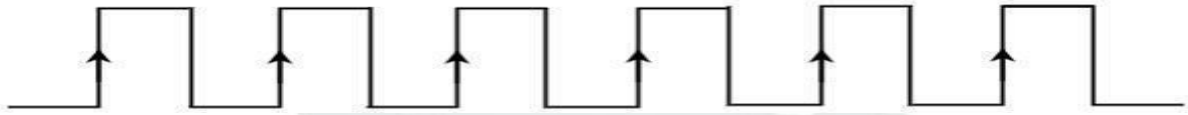
Edge triggering

There are two types of transitions that occur in clock signal. That means, the clock signal transitions either from Logic Low to Logic High or Logic High to Logic Low.

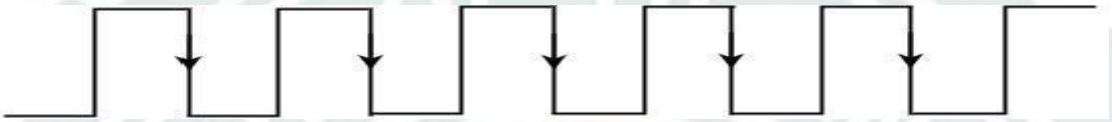
Following are the two **types of edge triggering** based on the transitions of clock signal.

- Positive edge triggering
- Negative edge triggering

If the sequential circuit is operated with the clock signal that is transitioning from Logic Low to Logic High, then that type of triggering is known as **Positive edge triggering**. It is also called as rising edge triggering. It is shown in the following figure.



If the sequential circuit is operated with the clock signal that is transitioning from Logic High to Logic Low, then that type of triggering is known as **Negative edge triggering**. It is also called as falling edge triggering. It is shown in the following figure.



There are two types of memory elements based on the type of triggering that is suitable to operate it.

- Latches
- Flip-flops

Latches operate with enable signal, which is **level sensitive**. Whereas, flip-flops are edge sensitive.

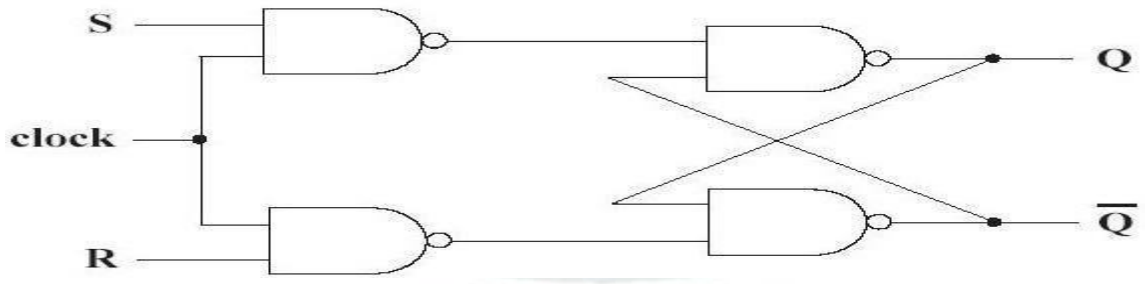
There are 4 types of flip flops:

- SR Flip-Flop
- D Flip-Flop
- JK Flip-Flop
- T Flip-Flop

SR Flip-Flop

SR flip-flop operates with only positive clock transitions or negative clock transitions. Whereas, SR latch operates with enable signal.

The **circuit diagram** of SR flip-flop is shown in the following figure.



This circuit has two inputs S & R and two outputs Q& Q'. The operation of SR flipflop is similar to SR Latch. But, this flip-flop affects the outputs only when positive transition of the clock signal is applied instead of active enable.

The following table shows the **state table** of SR flip-flop.

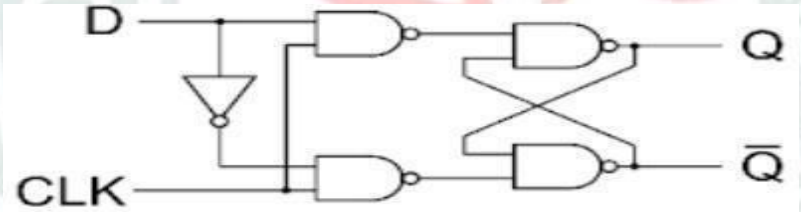
S	R	Qt+1
0	0	Q
0	1	0
1	0	1
1	1	-

Here, Q & Qt+1 are present state & next state respectively. So, SR flip-flop can be used for one of these three functions such as Hold, Reset & Set based on the input conditions, when positive transition of clock signal is applied.

D Flip-Flop

D flip-flop operates with only positive clock transitions or negative clock transitions. Whereas, D latch operates with enable signal. That means, the output of D flip-flop is insensitive to the changes in the input, D except for active transition of the clock signal.

The **circuit diagram** of D flip-flop is shown in the following figure.



This circuit has single input D and two outputs Q & Q'. The operation of D flip-flop is similar to D Latch. But, this flip-flop affects the outputs only when positive transition of the clock signal is applied instead of active enable.

The following table shows the **state table** of D flip-flop.

D	Qt + 1
0	0
1	1

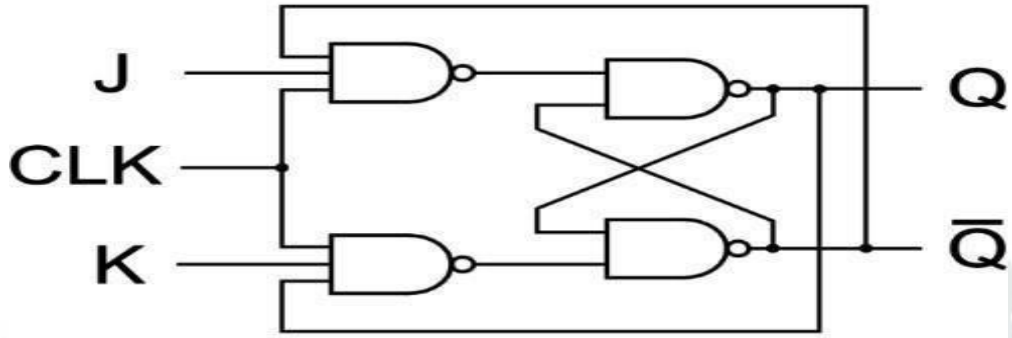
Therefore, D flip-flop always Hold the information, which is available on data input, D of earlier positive transition of clock signal.

D flip-flops can be used in registers, **shift registers** and some of the counters.

JK Flip-Flop

JK flip-flop is the modified version of SR flip-flop. It operates with only positive clock transitions or negative clock transitions.

The **circuit diagram** of JK flip-flop is shown in the following figure.



This circuit has two inputs J & K and two outputs Q & Q'. The operation of JK flip-flop is similar to SR flip-flop.

The following table shows the **state table** of JK flip-flop.

J	**K**	**Q**t+1
0	0	Q
0	1	0
1	0	1
1	1	Q'

Here, Q & Qt+1 are present state & next state respectively. So, JK flip-flop can be used for one of these four functions such as Hold, Reset, Set & Complement of present state based on the input conditions, when positive transition of clock signal is applied.

Master-Slave JK Flip Flop

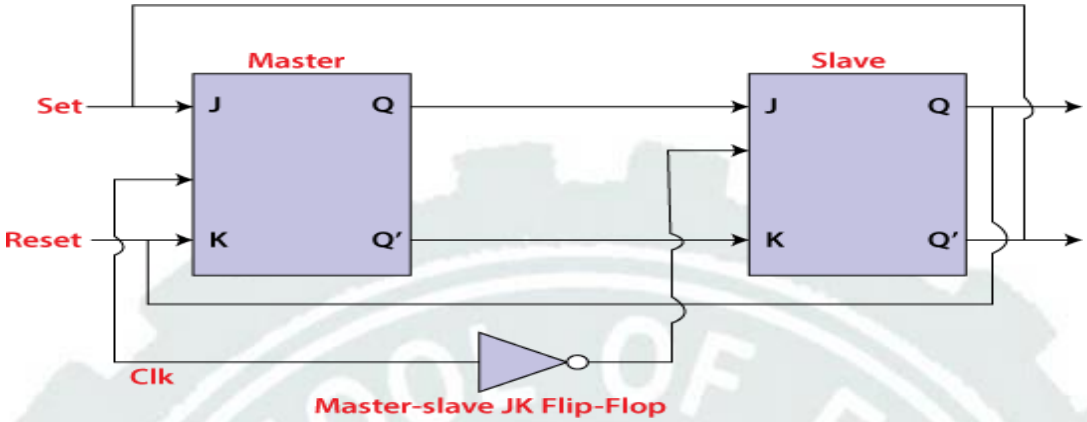
In "JK Flip Flop", when both the inputs and CLK set to 1 for a long time, then Q output toggle until the CLK is 1. Thus, the uncertain or unreliable output produces. This problem is referred to as a **race-round condition** in JK flip-flop and avoided by ensuring that the CLK set to 1 only for a very short time.

Explanation

The master-slave flip flop is constructed by combining two J K flip flop. These flip flops are connected in a series configuration. In these two flip flops, the 1st flip flop work as "master", called the master flip flop, and the 2nd work as a "slave", called slave flip flop.

In "master-slave flip flop", apart from these two flip flops, an inverter or NOT gate is also used. For passing the inverted clock pulse to the "slave" flip flop, the inverter is connected to the

clock's pulse. In simple words, when CP set to false for "master", then CP is set to true for "slave", and when CP set to true for "master", then CP is set to false for "slave".

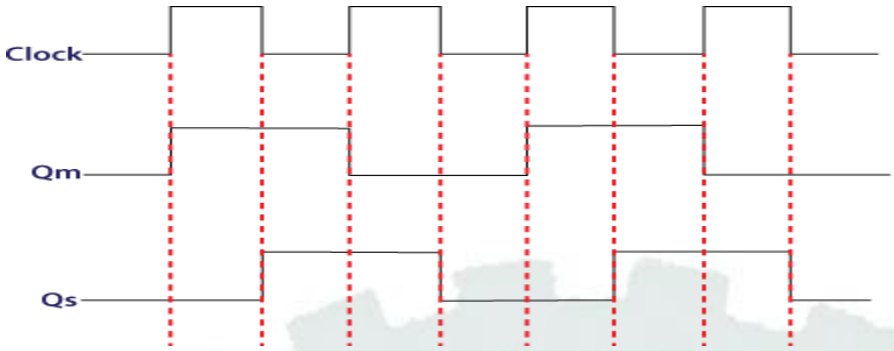


Master-slave JK Flip-Flop

Working:

- When the clock pulse is true, the slave flip flop will be in the isolated state, and the system's state may be affected by the J and K inputs. The "slave" remains isolated until the CP is 1. When the CP set to 0, the master flip-flop passes the information to the slave flip flop to obtain the output.
- The master flip flop responds first from the slave because the master flip flop is the positive level trigger, and the slave flip flop is the negative level trigger.
- The output Q'=1 of the master flip flop is passed to the slave flip flop as an input K when the input J set to 0 and K set to 1. The clock forces the slave flip flop to work as reset, and then the slave copies the master flip flop.
- When J=1, and K=0, the output Q=1 is passed to the J input of the slave. The clock's negative transition sets the slave and copies the master.
- The master flip flop toggles on the clock's positive transition when the inputs J and K set to 1. At that time, the slave flip flop toggles on the clock's negative transition.
- The flip flop will be disabled, and Q remains unchanged when both the inputs of the JK flip flop set to 0.

Timing Diagram of a Master Flip Flop:

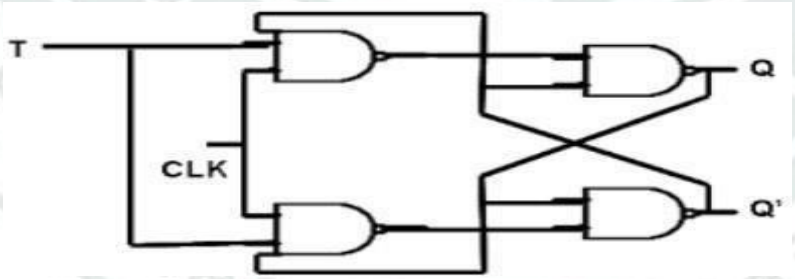


- When the clock pulse set to 1, the output of the master flip flop will be one until the clock input remains 0.
- When the clock pulse becomes high again, then the master's output is 0, which will be set to 1 when the clock becomes one again.
- The master flip flop is operational when the clock pulse is 1. The slave's output remains 0 until the clock is not set to 0 because the slave flip flop is not operational.
- The slave flip flop is operational when the clock pulse is 0. The output of the master remains one until the clock is not set to 0 again.
- Toggling occurs during the entire process because the output changes once in the cycle.

T Flip-Flop

T flip-flop is the simplified version of JK flip-flop. It is obtained by connecting the same input 'T' to both inputs of JK flip-flop. It operates with only positive clock transitions or negative clock transitions.

The **circuit diagram** of T flip-flop is shown in the following figure.



This circuit has single input T and two outputs Q & Q'. The operation of T flip-flop is same as that of JK flip-flop. Here, we considered the inputs of JK flip-flop as **J = T** and **K = T** in order to utilize the modified JK flip-flop for 2 combinations of inputs. So, we eliminated the other two combinations of J & K, for which those two values are complement to each other in T flipflop.

The following table shows the **state table** of T flip-flop.

D	**Q**t+1

0	Q
1	Q’

Here, Q & Qt+1 are present state & next state respectively. So, T flip-flop can be used for one of these two functions such as Hold, & Complement of present state based on the input conditions, when positive transition of clock signal is applied.
The output of T flip-flop always toggles for every positive transition of the clock signal, when input T remains at logic High 11. Hence, T flip-flop can be used in **counters**.

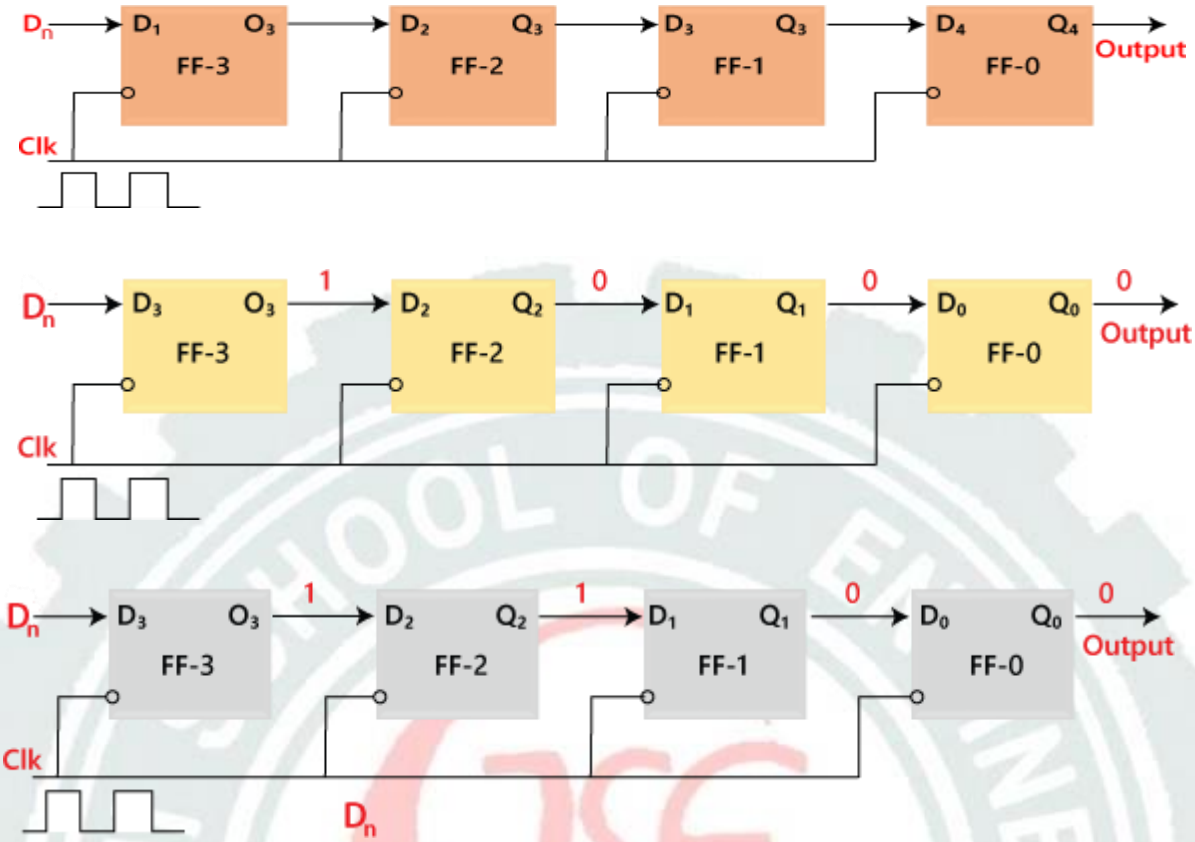
UNIT-4
Registers, memories and PLD
Shift register

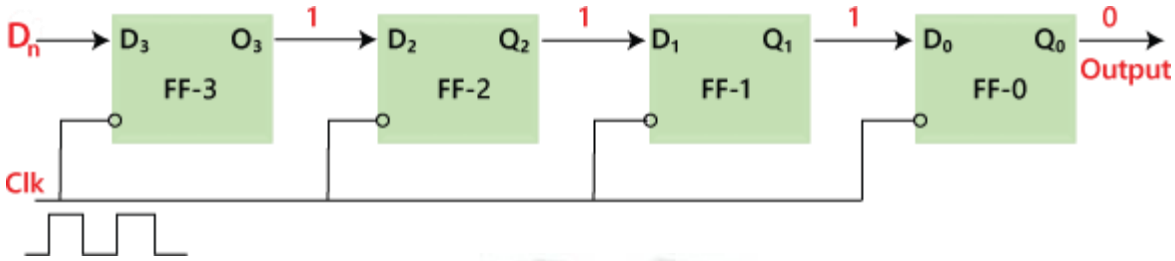
- Flip flops can be used to store a single bit of binary data (1or 0).
- However, in order to store multiple bits of data, we need multiple flip flops. N flip flops are to be connected in an order to store n bits of data.
- A **Register** is a device which is used to store such information. It is a group of flip flops connected in series used to store multiple bits of data.
- The information stored within these registers can be transferred with the help of **shift registers**.
- Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses.
- An n-bit shift register can be formed by connecting n flip-flops where each flip flop stores a single bit of data.

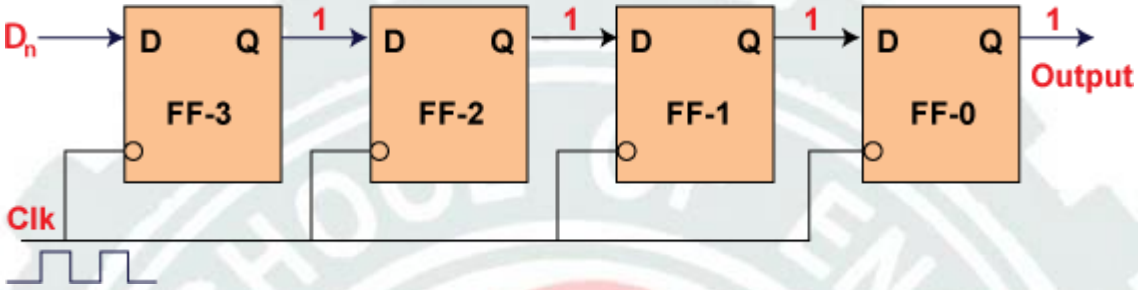
Shift registers are basically of 4 types. These are:

1. Serial In Serial Out shift register
2. Serial In parallel Out shift register
3. Parallel In Serial Out shift register
4. Parallel In parallel Out shift register

Serial-In Serial-Out Shift Register (SISO) –
The shift register, which allows serial input (one bit after the other through a single data line) and produces a serial output is known as Serial-In Serial-Out shift register. Since there is only one output, the data leaves the shift register one bit at a time in a serial pattern, thus the name Serial-In Serial-Out Shift Register. The circuit consists of four D flip-flops which are connected in a serial manner. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop. The main use of a SISO is to act as a delay element.

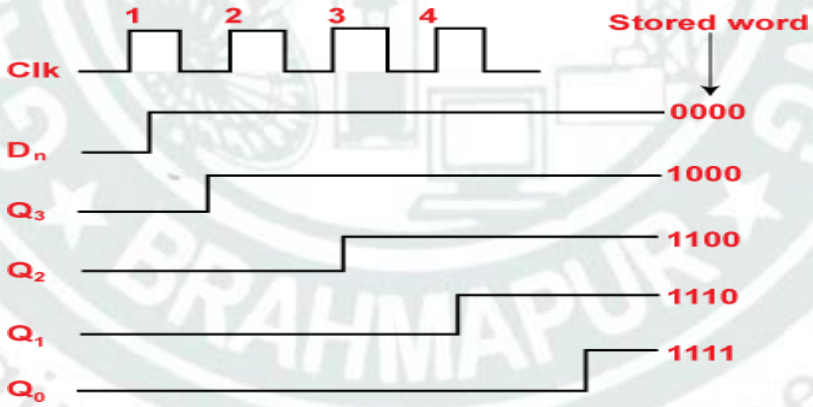

Dn
D1
O3
FF-3
D2
Q3
FF-2
D3
Q3
FF-1
D4
Q4
FF-0
Output
Clk
Dn
D3
O3
FF-3
1
D2
Q2
FF-2
0
D1
Q1
FF-1
0
D0
Q0
FF-0
0
Output
Clk
Dn
D3
O3
FF-3
1
D2
Q2
FF-2
1
D1
Q1
FF-1
0
D0
Q0
FF-0
0
Output
Clk
Dn





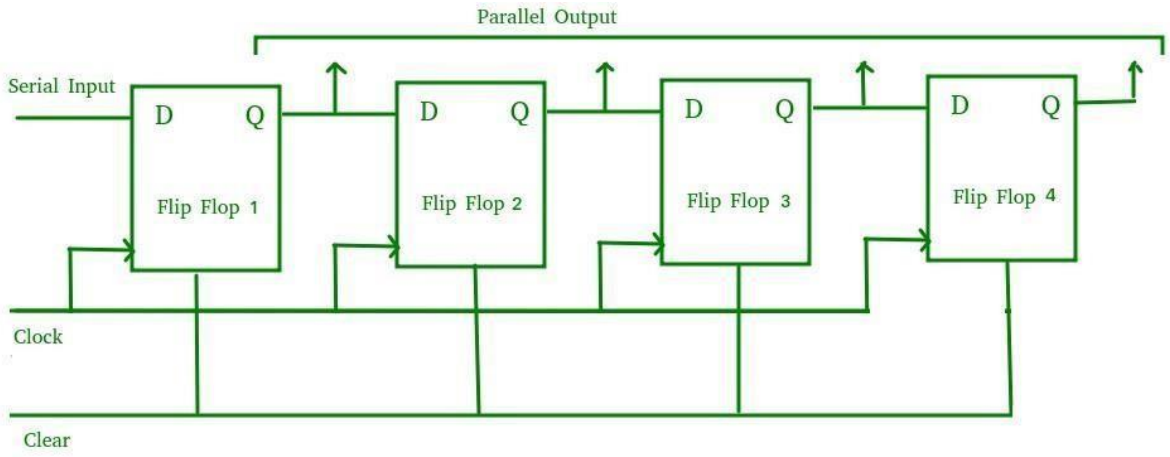
	Clk	$D_n=Q_3$	$Q_3=D_2$	$Q_2=D_1$	$Q_1=D_0$	Q_0
Initially			0	0	0	0
(1)	↓	1	1	0	0	0
(2)	↓	1	1	1	0	0
(3)	↓	1	1	1	1	0
(4)	↓	1	1	1	1	1

→ Direction of data travel



Serial-In Parallel-Out shift Register (SIPO) –

The shift register, which allows serial input (one bit after the other through a single data line) and produces a parallel output is known as Serial-In Parallel-Out shift register. The circuit consists of four D flip-flops which are connected. The clear (CLR) signal is connected in addition to the clock signal to all the 4 flip flops in order to RESET them. The output of the first flip flop is connected to the input of the next flip flop and so on. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop. They are used in communication lines where demultiplexing of a data line into several parallel lines is required because the main use of the SIPO register is to convert serial data into parallel data.



Parallel IN Serial OUT (PISO)

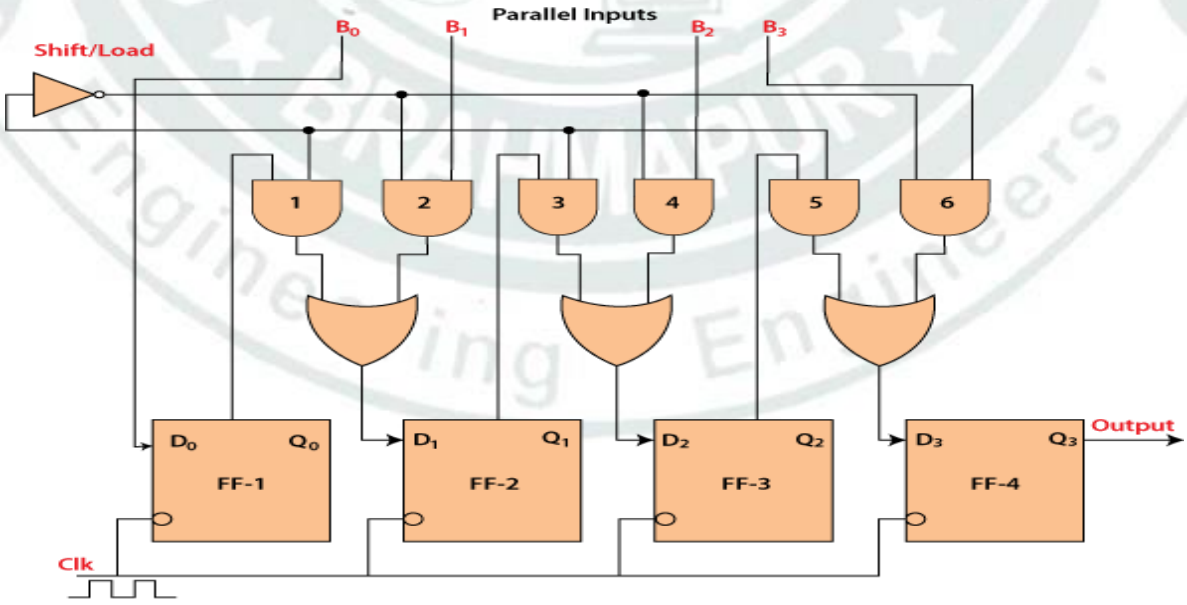
In the **"Parallel IN Serial OUT"** register, the data is entered in a parallel way, and the outcome comes serially. A four-bit **"Parallel IN Serial OUT"** register is designed below. The input of the flip flop is the output of the previous Flip Flop. The input and outputs are connected through the combinational circuit. Through this combinational circuit, the binary input B_0, B_1, B_2, B_3 are passed. The **shift mode** and the **load mode** are the two modes in which the **"PISO"** circuit works.

Load mode

The bits B_0, B_1, B_2, and B_3 are passed to the corresponding flip flops when the second, fourth, and sixth "AND" gates are active. These gates are active when the shift or load bar line set to 0. The binary inputs B0, B1, B2, and B3 will be loaded into the respective flip-flops when the edge of the clock is low. Thus, parallel loading occurs.

Shift mode

The second, fourth, and sixth gates are inactive when the load and shift line set to 0. So, we are not able to load data in a parallel way. At this time, the first, third, and fifth gates will be activated, and the shifting of the data will be left to the right bit. In this way, the **"Parallel IN Serial OUT"** operation occurs.

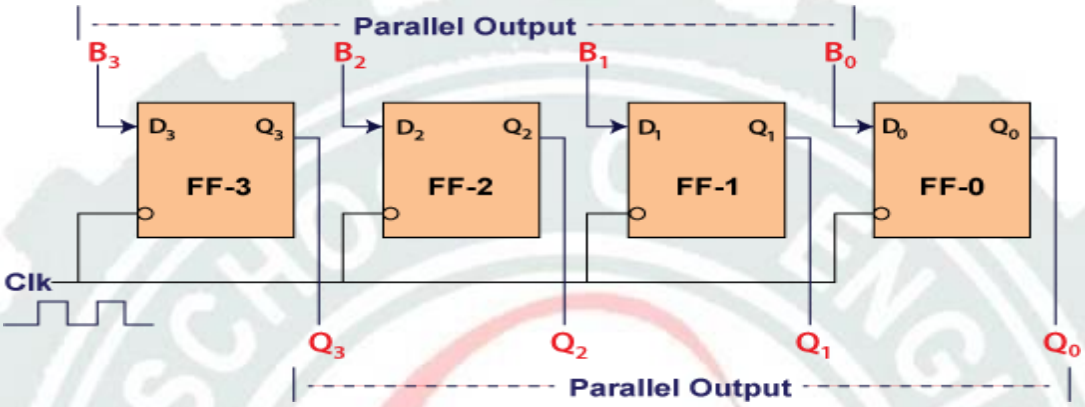


A Parallel in Serial out (PISO) shift register us used to convert parallel data to serial data.

Parallel IN Parallel OUT (PIPO)

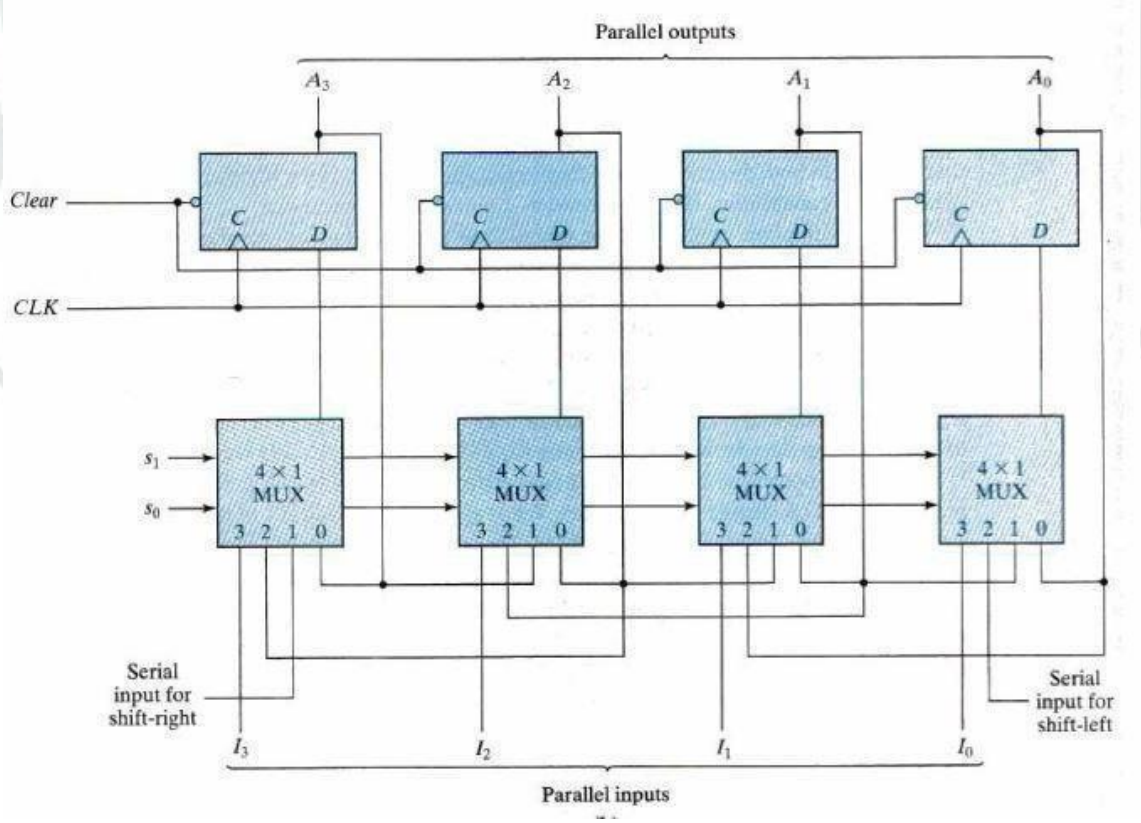
In **"Parallel IN Parallel OUT"**, the inputs and the outputs come in a parallel way in the register.

The inputs A_0, A_1, A_2, and A_3, are directly passed to the data inputs D_0, D_1, D_2, and D_3 of the respective flip flop. The bits of the binary input is loaded to the flip flops when the negative clock edge is applied. The clock pulse is required for loading all the bits. At the output side, the loaded bits appear.



Universal shift register

A Universal shift register is a register which has both the right shift and left shift with parallel load capabilities. Universal shift registers are used as memory elements in computers. A Unidirectional shift register is capable of shifting in only one direction. A bidirectional shift register is capable of shifting in both the directions. The Universal shift register is a combination design of **bidirectional** shift register and a **unidirectional** shift register with parallel load provision



Basic connections –

1. The first input (zeroth pin of multiplexer) is connected to the output pin of the corresponding flip-flop.
2. The second input (first pin of multiplexer) is connected to the output of the veryprevious flip flop which facilitates the right shift.
3. The third input (second pin of multiplexer) is connected to the output of the very-next flip-flop which facilitates the left shift.
4. The fourth input (third pin of multiplexer) is connected to the individual bits of the input data which facilitates parallel loading.

The working of the Universal shift register depends on the inputs given to the select lines.

The register operations performed for the various inputs of select lines are as follows:

S1	S0	Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

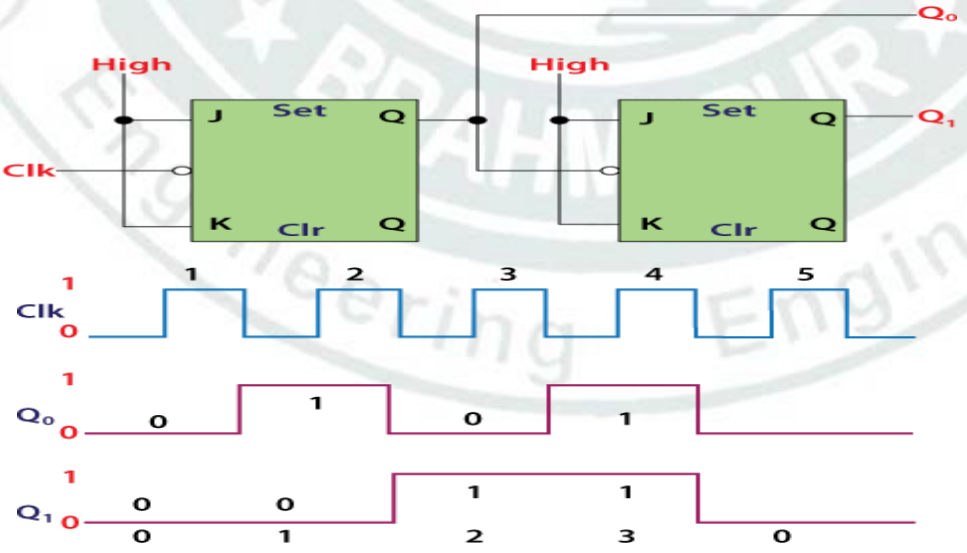
Counters

Counter is a sequential circuit. A digital circuit which is used for a counting pulses is known counter. Counter is the widest application of flip-flops. It is a group of flip-flops with a clock signal applied. Counters are of two types.

- Asynchronous or ripple counters. Synchronous counters.

Asynchronous or ripple counters

The **Asynchronous counter** is also known as the **ripple counter**. Below is a diagram of the 2-bit **Asynchronous counter** in which we used two T flip-flops or two JK flip flopby setting both of the inputs to 1 permanently. The external clock pass to the clock input of the first flip flop, i.e., FF-A and its output, i.e., is passed to clock input of the next flip flop, i.e., FF-B.



Operation:

1. **Condition 1:** When both the flip flops are in reset condition.
   Operation: The outputs of both flip flops, i.e., Q_A Q_B, will be 0.
2. **Condition 2:** When the first negative clock edge passes.
   Operation: The first flip flop will toggle, and the output of this flip flop will change from 0 to 1. The output of this flip flop will be taken by the clock input of the next flip flop. This output will be taken as a positive edge clock by the second flip flop. This input will not change the second flip flop's output state because it is the negative edge triggered flip flop. So, $Q_A = 1$ and $Q_B = 0$
3. **Condition 3:** When the second negative clock edge is applied.
   Operation: The first flip flop will toggle again, and the output of this flip flop will change from 1 to 0. This output will be taken as a negative edge clock by the second flip flop. This input will change the second flip flop's output state because it is the negative edge triggered flip flop. So, $Q_A = 0$ and $Q_B = 1$.
4. **Condition 4:** When the third negative clock edge is applied.
   Operation: The first flip flop will toggle again, and the output of this flip flop will change from 0 to 1. This output will be taken as a positive edge clock by the second flip flop. This input will not change the second flip flop's output state because it is the negative edge triggered flip flop. So, $Q_A = 1$ and $Q_B = 1$
5. **Condition 5:** When the fourth negative clock edge is applied.
   Operation: The first flip flop will toggle again, and the output of this flip flop will change from 1 to 0. This output will be taken as a negative edge clock by the second flip flop. This input will change the output state of the second flip flop. So, $Q_A = 0$ and $Q_B = 0$

Classification of counters

Depending on the way in which the counting progresses, the synchronous or asynchronous counters are classified as follows −

- Up counters
- Down counters
- Up/Down counters

UP/DOWN Counter

Up counter and down counter is combined together to obtain an UP/DOWN counter. A mode control (M) input is also provided to select either up or down mode. A combinational circuit is required to be designed and used between each pair of flip-flop in order to achieve the up/down operation.

- Type of up/down counters
- UP/DOWN ripple counters
- UP/DOWN synchronous counter

UP/DOWN Counter

Up counter and down counter is combined together to obtain an UP/DOWN counter. A mode control (M) input is also provided to select either up or down mode. A combinational circuit is

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- Type of up/down counters
- UP/DOWN ripple counters
- UP/DOWN synchronous counter

UP/DOWN Ripple Counters

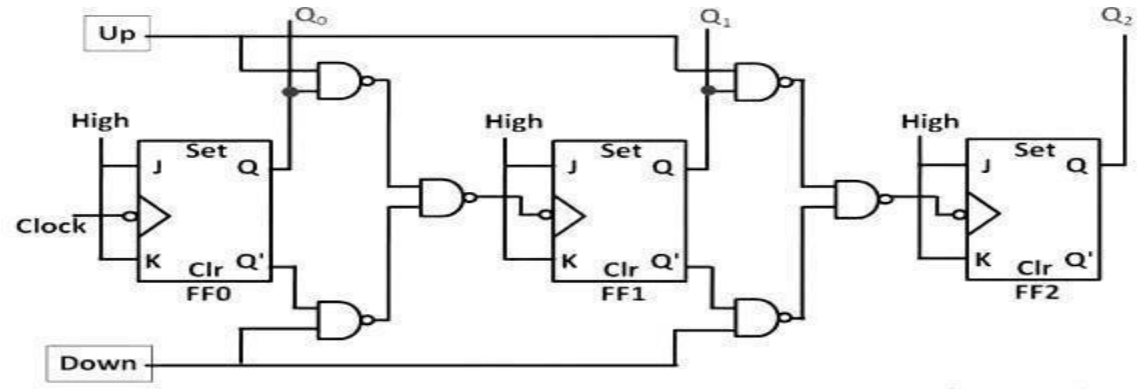
In the UP/DOWN ripple counter all the FFs operate in the toggle mode. So, either T flip-flops or JK flip-flops are to be used. The LSB flip-flop receives clock directly. But the clock to every other FF is obtained from (Q = Q bar) output of the previous FF.

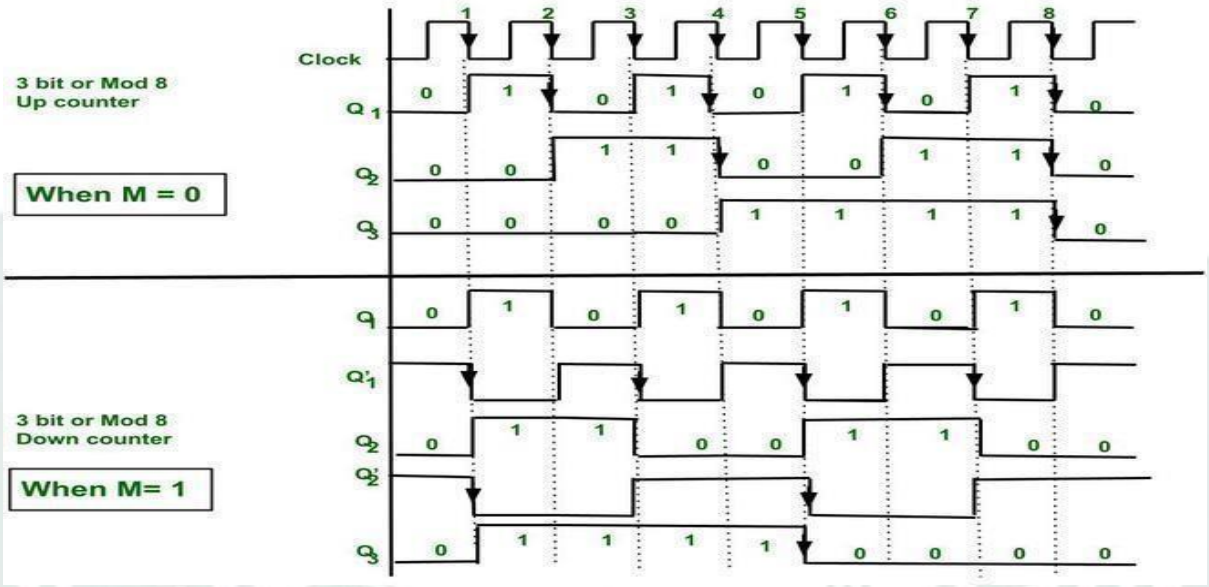
- **UP counting mode (M=0)** − The Q output of the preceding FF is connected to the clock of the next stage if up counting is to be achieved. For this mode, the mode select input M is at logic 0 (M=0).
- **DOWN counting mode (M=1)** − If M = 1, then the Q bar output of the preceding FF is connected to the next FF. This will operate the counter in the counting mode.

Example

3- bit binary up/down ripple counter.

- 3-bit − hence three FFs are required.
- UP/DOWN − So a mode control input is essential.
- For a ripple up counter, the Q output of preceding FF is connected to the clock input of the next one.
- For a ripple up counter, the Q output of preceding FF is connected to the clock input of the next one.
- For a ripple down counter, the Q bar output of preceding FF is connected to the clock input of the next one.
- Let the selection of Q and Q bar output of the preceding FF be controlled by the mode control input M such that, If M = 0, UP counting. So, connect Q to CLK. If M = 1, DOWN counting. So, connect Q bar to CLK.





Modulus Counter (MOD-N Counter)

The 2-bit ripple counter is called as MOD-4 counter and 3-bit ripple counter is called as MOD8 counter. So, in general, an n-bit ripple counter is called as modulo-N counter. Where, MOD number = 2^n.

Type of modulus

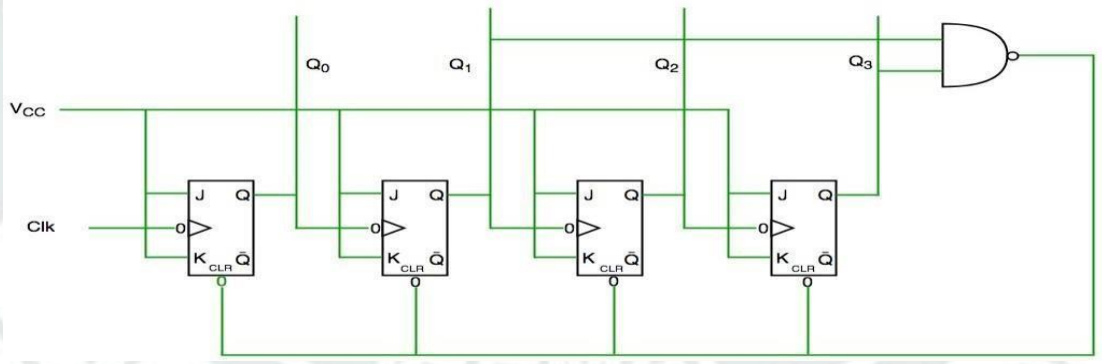
- 2-bit up or down (MOD-4)
- 3-bit up or down (MOD-8)
- 4-bit up or down (MOD-16) **Application of counters**
- Frequency counters
- Digital clock
- Time measurement
- A to D converter
- Frequency divider circuits
- Digital triangular wave generator.

Decade counter

A decade counter counts ten different states and then reset to its initial states. A simple decade counter will count from 0 to 9 but we can also make the decade counters which can go through any ten states between 0 to 15 (for 4 bit counter).

Clock pulse Q3 Q2 Q1 Q0

0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0



We see from circuit diagram that we have used NAND gate for Q3 and Q1 and feeding this to clear input line because binary representation of 10 is–1010

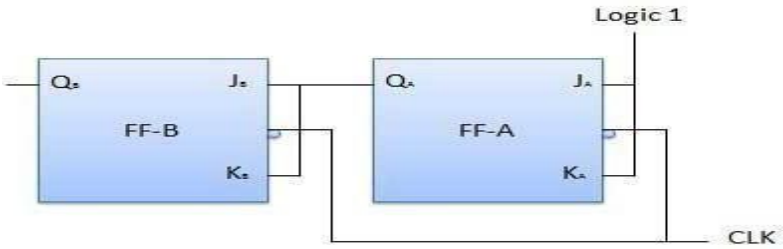
And we see Q3 and Q1 are 1 here, if we give NAND of these two bits to clear input then counter will be clear at 10 and again start from beginning.

Synchronous counters

If the "clock" pulses are applied to all the flip-flops in a counter simultaneously, then such a counter is called as synchronous counter.

2-bit Synchronous up counter

The J_A and K_A inputs of FF-A are tied to logic 1. So, FF-A will work as a toggle flip-flop. The J_B and K_B inputs are connected to Q_A.

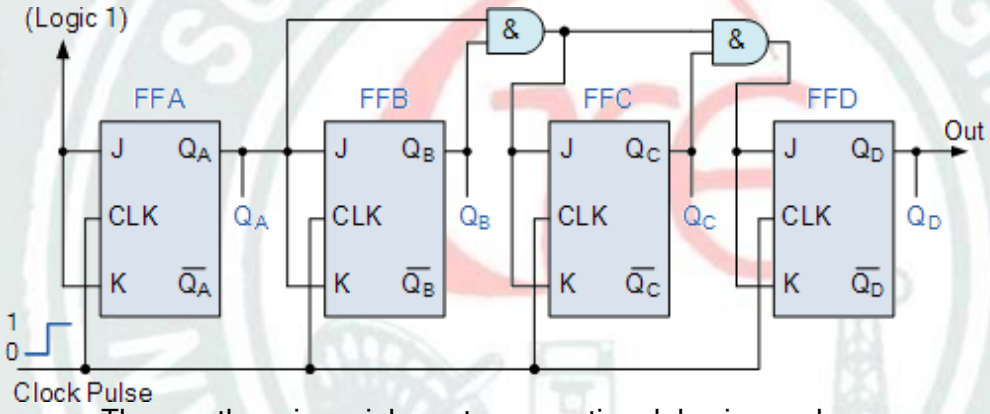


Operation

S.N.	Condition	Operation
1	**Initially let both the FFs be in the reset state**	Q_BQ_A = 00 initially.
2	**After 1st negative clock edge**	As soon as the first negative clock edge is applied, FF-A will toggle and Q_A will change from 0 to 1. But at the instant of application of negative clock edge, Q_A , $J_B = K_B = 0$. Hence FF-B will not change its state. So Q_B will remain 0. Q_BQ_A = 01 after the first clock pulse.
3	**After 2nd negative clock edge**	On the arrival of second negative clock edge, FF-A toggles again and Q_A changes from 1 to 0. But at this instant Q_A was 1. So $J_B = K_B$= 1 and FF-B will toggle. Hence Q_B changes from 0 to 1. Q_BQ_A = 10 after the second clock pulse.
4	**After 3rd negative clock edge**	On application of the third falling clock edge, FF-A will toggle from 0 to 1 but there is no change of state for FF-B. Q_BQ_A = 11 after the third clock pulse.
5	**After 4th negative clock edge**	On application of the next clock pulse, Q_A will change from 1 to 0 as Q_B will also change from 1 to 0. Q_BQ_A = 00 after the fourth clock pulse.

4- bit synchronous counter

- The external clock pulses (pulses to be counted) are fed directly to each of the J-K flipflops in the counter chain and that both the J and K inputs are all tied together in toggle mode, but only in the first flip-flop, flip-flop FFA (LSB) are they connected HIGH, logic
  "1" allowing the flip-flop to toggle on every clock pulse.
- Then the synchronous counter follows a predetermined sequence of states in response to the common clock signal, advancing one state for each pulse.
- The J and K inputs of flip-flop FFB are connected directly to the output Q_A of flipflop FFA, but the J and K inputs of flip-flops FFC and FFD are driven from separate AND gates which are also supplied with signals from the input and output of the previous stage.
- These additional AND gates generate the required logic for the JK inputs of the next stage.
- If we enable each JK flip-flop to toggle based on whether or not all preceding flip-flop outputs (Q) are "HIGH" we can obtain the same counting sequence as with the asynchronous circuit but without the ripple effect, since each flip-flop in this circuit will be clocked at exactly the same time.



- Then as there is no inherent propagation delay in synchronous counters, because all the counter stages are triggered in parallel at the same time, the maximum operating frequency of this type of frequency counter is much higher than that for a similar asynchronous counter circuit.

UNIT-5
A/D and D/A Converters

Necessity of A/D and D/A converters.

A digital quantity will have a value that is specified as one of two possibilities such as 0 or

A digital quantity will have a value that is specified as one of two possibilities such as 0 or 1, LOW or HIGH, true or false, and so on. In practice, the voltage representation a digital quantity such as a mayactually have a value that is anywhere within specified ranges. For example, for TTL logic :

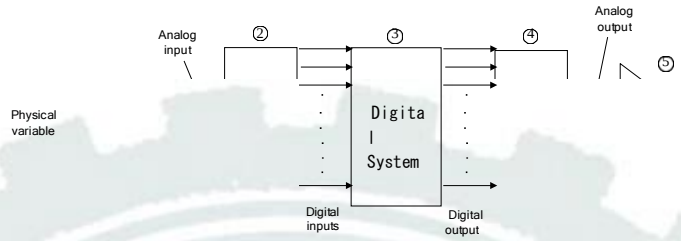
0V to 0.8V = logic
02V to 5V = logic
1

Any voltage falling in the range 0 to 0.8 V is given the digital value 0, and any voltage in the range 2 to 5 V is assigned the digital value 1. The digital circuits respond accordingly to all voltage values within a given range.

Most physical variables are analog in nature and can take on any value within a continuous range of values.

Most physical variables are analog in nature and can take on any value within a continuous range of values. Examples include temperature, pressure, light intensity, audio signals, position, rotational speed, and flow rate. Digital systems perform all of their internal operations using digital circuitry and digital operations. Any information that has to be inputted to a digital system must first be put into digital form. Similarly, the outputs from a digital system are always in digital form.

Note that the transducer's output is directly proportional to temperature; such that each 1 ^{0}F produces a 10mV output. Analog-to-
digital converter (ADC) and digital-to-converter (DAC) are used to interface a computer to the analog world so that the computer can monitor and control a physical variable Fig. 7.1.



This digital output from the computer is connected to a DAC, which converts it to a proportional analog voltage or current.

Digital-to-Analog Converter (DAC)

This digital output from the computer is connected to a DAC, which converts it to a proportional analog voltage or current. For example, the computer might produce a digital output ranging from 0000000 to 11111111, which the DAC converts to a voltage ranging from 0 to 10V.

Fig. 7.2 : Four bit DAC with voltage output.

.

In general,
Analog output = K × digital input

where K is the proportionality factor and it is constant value for a given DAC. The analog output can of course be a voltage or current. When it is a voltage, K will be in voltage units, and when the output is current, K will be in current units. For the DAC of K=1 V, so that

V_{OUT} = (1 V) × digital input

We can use this to calculate V_{OUT} for any value of digital input. For example, with a digital input of $1100_2 = 12_{10}$, we obtain

V_{OUT} = 1V × 12 = 12V

Problem 1 and Solution

Problem 1

A 5-bit DAC has a current output. For a digital input of 101000, an output current of 10mA is produced. What will IOUT be for a digital input of 11101?

Solution

The digital input 10100_2 is equal to decimal 20. Since I_{OUT} = 10 mA for this case, the proportionality factor as 0.5 mA. Thus, we can find for a digital input such as $11101_2 = 29_{10}$ as follows :

I_{OUT} = (0.5mA) × 29
= 14.5 mA

Remember, the proportionality factor, K, will vary from one DAC to another.

Problem 2

What is the largest value of output voltage from an 8-bit DAC that produces 1.0V for a digital input of 00110010?

Solution

$00110010_2 = 50_{10}$
1.0 V = K× 50

Therefore
, K = 20
mV

The largest output will occur for an input of 11111111_2 =

$255_{10}.V_{OUT}$(max) = 20mV×255
= 5.10 V

Analog Output

Analog Output

The output of a DAC is technically not an analog quantity because it can take on only specific values like the 16 possible voltage levels for Vout. Thus, in that sense, it is actually digital. However, the number of different possible output levels can be increased and the difference between successive values can be decreased by increasing the number of input bits. This will allow us to produce an output that is more and more like an analog quantity that varies continuously over a range of values.

Input Weights

For the DAC of it should be noted that each digital input contributes a different amount to the analog output. This is easily seen if we examine the cases where only one input is HIGH Table 7.1. The contributions of each digital input are weighted according to their position in the binary number.

D	C	B	A		V_{OUT} (V)
0	0	0	1	→	1
0	0	1	0	→	2
0	1	0	0	→	4
1	0	0	0	→	8

Table 7.1

Thus, A, which is the LSB, has a weight of 1V, B has a weight of 2V, C has a weight of 4 V, and D, the MSB, has the largest weight 8V. The weights are successively doubled for each bit, beginning with the LSB. Thus, we can consider V_{OUT} to be the weighted sum of the digital inputs. For instance, to find V_{OUT} for the digital input 0111 we can add the weights of the C, B, and A bits to obtain 4 V + 2V + 1V=7V.

Problem 3

Input Weights Problem 3 and Solution

A 5-bit D/A converter produces V_{OUT} = 0.2 V for a digital input of 0001. Find the value of Vout for an input of 11111.

Solution

Obviously, 0.2 V is the weight of the LSB. Thus, the weights of the other bits must be 0.4 V, 0.8 V, 1.6 V, and 3.2 V respectively. For a digital input of 11111, then, the value of V_{OUT} will be 3.2 V + 1.6 V+ 0.8V + 0.4V + 0.2 V = 6.2 V.

Resolution

Resolution of a D/A converter is defined as the smallest change that can occur in he analog output as a result of a change in the digital input

Resolution of a D/A converter is defined as the smallest change that can occur in he analog output as a result of a change in the digital input. We can see that the resolution is 1V, since V_{OUT} can change by no less than 1 V when the digital input value is changed. The resolution is always equal to the weight of the LSB and is also referred to as the step size. As the counter is being continually cycled through its 16 states by the clock signal, the DAC output is a staircase waveform that goes up 1 V per step. When the counter is at 1111, the DAC output is at its maximum value of 15 V; this is its full-scale output. When the counter recycles to

0000, the DAC output returns to 0V. The resolution or step size of thejumps in the staircase waveform; in this case, each step is 1 V.

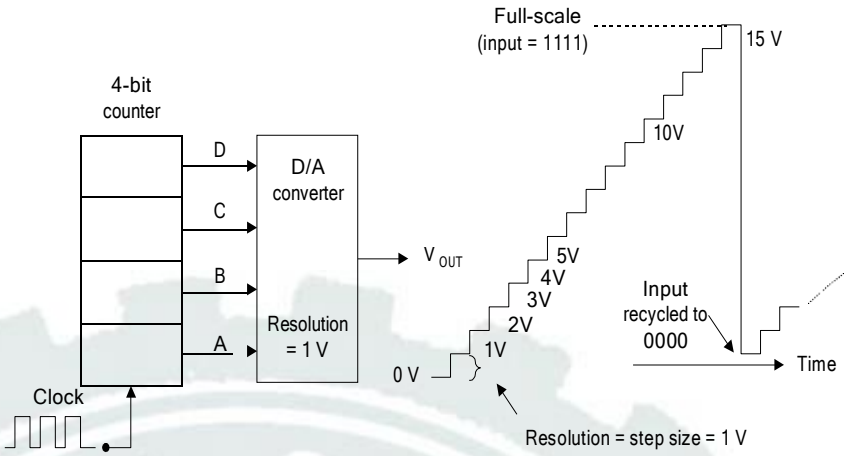


Fig. 7.3 : Output wave forms of a four bit DAC.

Note that the staircase has 16 levels corresponding to the 16 input states,but there are only 15 steps or jumps between the 0-V level and full-scale,

In general, for an N-bit DAC the number of different levels will be 2^N, and the number of steps will be $2^N - 1$.

You may have already figured out the resolution (step size) is the same as the proportionality factor in the DAC input/output relationship :

analog output = K × digital input

A new interpretation of this expression would be that the digital input is equal to the number of the step, K is the amount of voltage (or current) per step, and the analog output is the product of the two.

Problem 4

For the DAC of Example 3 determine V_{OUT} for a digital input of 10001.

Solution

The step size is 0.2 V, which is the proportionality factor K. The digital input is $10001 = 17_{10}$. Thus we have :

$V_{OUT} = (0.2\ V) \times 17$
$= 3.4V$

Percentage Resolution

Although resolution can be expressed as the amount of voltage or current per step, it is also useful to express it as a percentage of the full-scale output. To illustrate, in Fig. 7.3 the DAC has a maximum full-scale output of 15 V (when the digital input is 1111). The step size is 1V, which gives a percentage resolution.

$$\%\ resolution = \frac{\text{step size}}{full\ scale\ (F.S.)} \times 100\%$$

$$= \frac{1V}{15V} \times 100\% = 6.67\%$$

Percentage Resolution Problem 5 and Solution

Problem 5

A 10-bit DAC has a step size of 10 mV. Determine the full-scale outputvoltage and the percentage resolution.

Solution

With 10 bits, there will be 2 - 1 = 1023 steps of 10mV each. The full-scale output will therefore be 10mV × 1023 = 10.23 V and

$$\%\ resolution = \frac{10\ mV}{10.23\ V} \times 100\% \approx 0.1\%$$

Problem 4 helps to illustrate the fact that the percentage resolution becomes smaller as the number of input bits is increased. In fact, the percentage resolution can also be calculated from.

$$\%\ resolution = \frac{1}{\text{total number of steps}} \times 100\%$$

For an N-bit binary input code the total number of steps is 2 -1. Thus,for the previous example,

$$\%\ resolution = \frac{1}{2^{10} - 1} \times 100\%$$

$$= \frac{1}{1023} \times 100\%$$

$$\approx 0.1\%$$

This means that it is only the number of bits which determines the percentage resolution. Increase of the number of bits increases the number of steps to reach full scale.

Exercise

Multiple choice questions

D/A Converter

The purpose of a digital-to-analog converter is to convert a binary word to a proportional current or voltage.

The purpose of a digital-to-analog converter is to convert a binary wordto a proportional current or voltage.

The binary weighted resistors produce binary-weighted current which are summed up by the op-amp to produce proportional output voltage. The binary word applied to the switches produces a proportional output voltage.

Several different binary codes such as straight binary, BCD and offset binary are commonly used as inputs to D/A converters.

D/A-Converter Circuitry

D/A-Converter Circuitry

There are several methods and circuits for producing the D/A operation. We shall examine several of the basic schemes, to gain an insight into the ideas used.

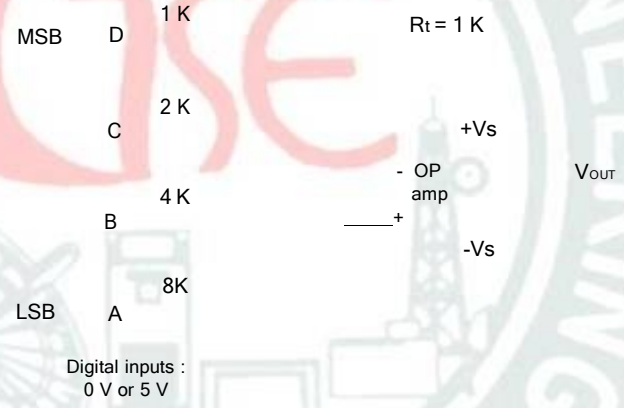


Fig. 7.4 : DAC circuitry using op-amp with binary weighted resistors.

Fig. 7.4 shows the basic circuit of 4-bit DAC. The inputs A,B,C, and D are binary inputs which are assumed to have values of either 0 V or 5 V. The operational amplifier is employed as a summing amplifier, which produces

the weighted sum of these input voltages. the summing amplifier multiplies each input voltage by the ratio of the feedback resistor R_F to the corresponding input resistor R_{IN}. In this circuit R_F R_{IN} 1kΩ and the input resistors range from 1 to 8 kΩ . The D input has R_{IN} = 1KΩ, so the summing amplifier passes the voltage at D with no attenuation. The C input has R_{IN} =
2 kΩ, so that it will be attenuated by. Similarly, the B input will be
attenuated by ¼ and the A input by $^1/_8$. The amplifier output can thus be
expressed as

$$V_{OUT} = - (V_D + {}^1/_2\ V_C + ¼\ V_B + {}^1/_8\ V_A)$$

The negative sign is present because the summing amplifier is a polarity- inverting amplifier, but it will but concern us here.

Clearly, the summing amplifier output is an analog voltage which represents a weighted sum of the digital inputs. The output is evaluated for any input condition by setting the appropriate inputs to either 0 V or 5 V. For example, if the digital input is 1010, then V_D = V_B = 5V and V_C = V_A = 0V. Thus, using equation

$$V_{OUT} = - (5V + OV + ¼ \times 5V + OV)$$
$$= - 6.25V$$

The resolution of this D/A converter is equal to the weighting of the ISB,
which is $^1/_8 \times 5V = 0.625$ V. The analog output increases by 0.625 V as the
binary input number advances one step.

Problem 6

Problem 6

Assume V_{REF} = 10 V and R = R = 10 kΩ. Determine the resolution and full- scale output for this DAC. Assume that R_L is much smaller than R.

Solution

$I_0 = V_{REE}/R$ = 1 mA. This is the weight of the MSB. The other three currents will be 0.5, 0.25, and 0.125 mA. The LSB is 0.125 mA, which is also the resolution.

The full-scale output will occur when the binary inputs are all HIGH so that each current switch is closed and

$$I_{OUT} = 1 + 0.5 + 0.25 + 0.125 = 1.875 \text{ mA}$$

Note that the output current is proportional to V_{REF}. If V_{REF} is increased or decreased, the resolution and full-scale output will change proportionally.

R/2R Ladder

R/2R Ladder

The DAC circuits we have looked at, has some practical limitations. The biggest problem is the large difference in resistor values between the LSB and MSB, especially in high-resolution DACs. One of the most widely used DAC circuits that uses resistance's fairly close in value is the R/2R ladder network. Here the resistance values span a range of only 2 to 1.

Note, how the resistors are arranged, and only two different values are used, R and 2R. The current I_{OUT} depends on the positions of the four switches, and the binary inputs $B_3B_2B_1B_0$ control the states of the switches. Thiscurrent is allowed to flow through an op-amp current-to-voltage converter to develop V_{OUT}. It can be shown that the value of V_{OUT} is given by theexpression.

$$V_{OUT} = \frac{REF}{8} \times B.$$

where B is the value of the binary input, which can range from 000 (0) to1111 (15).

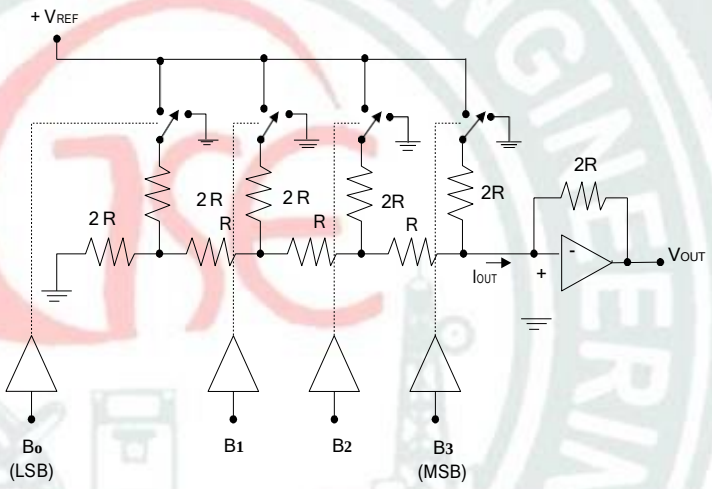


Fig. 7.5 : R/2R ladder DAC.

Accuracy

There are several ways of specifying accuracy. The two most common are called full-scale error and linearity error. which are normally expressed as a percentage of the converter's full-scale output (%F.S.)

Full-scale error is the maximum deviation of the DAC's output from its expected (ideal) value, expressed as a percentage of full scale. For example, assume that the DCA has an accuracy of ± 0.01% F.S. Since this converter has a full-scale output of 9.375 V, this percentage convertsto

$$\pm 0.01\% \times 9.375\ V = \pm 0.9375\ mV$$

This means that the output of this DAC can, at any time, be off by as much as 0.9375mV from its expected value.

Linearity error is the maximum deviation in step size from the ideal step size. For example, the DAC has an expected step size of 0.625 V. If this converter has a linearity error of ± 0.01F.S,, this would mean that the actual step size could be off by as much as 0.9375 mV.

Problem 7

Example 7 and Solution

A certain 8-bit DAC has a full-scale output of 2mA and a full-scale error of ± 0.5% F.S. What is the range of possible outputs for an input of 10000000?

Solution

The step size is 2mA/255 = 7.84 µA. Since $10000000 = 128_{10}$, the ideal output should be 128 × 7.84 µA. The error can be as much as

$$\pm 0.5\% \times 2mA = \pm 10\mu A$$

Thus, the actual output can deviate by this amount from the ideal 1004µA , so the actual output can be anywhere from 994 to 1014 µA.

Offset Error

Offset Error

Ideally, the output of a DAC will be zero volts when the binary input is all 0's. In practice, however, there will be a very small output voltage for this situation; this is called offset error. This offset error, if not corrected, will be added to the expected DAC output for all input cases. Offset error can be negative as well as positive.

Many DACs will have an external offset adjustment that allows you to zero the offset. This is usually accomplished by applying all 0s to the DAC input and monitoring the output while an offset adjustment potentiometer is adjusted until the output is as close to 0 V as required.

Settling Time

Settling Time

The operating speed of a DAC is usually specified by giving its settling time, which is the time required for the DAC output to go from zero to full scale as the binary input is changed from all 0's to all 1's. Typical values for settling time range from 50 ns to 10 μs.

Monotonicity

A DAC is monotonic if its output increases as the binary input is incremented from one value to the next. Another way to describe this is that the staircase output will have no downward steps as the binary input is incremented from zero to full scale.

Monotonicity
DAC
Applications
Control

DAC Applications

DACs are used whenever the output of a digital circuit has to provide an analog voltage or current to drive an analog device. Some of the most common applications are described in the following paragraphs.

Control

The digital output from a computer can be converted to an analog control signal to adjust the speed of a motor or the temperature of a furnace, to control almost any physical variable.

Automatic Testing

Automatic Testing
Signal

Computers can be programmed to generate the analog signals (through a DAC) needed to test analog circuitry. The test circuit's analog output response will normally be converted to a digital value by an ADC and fed into the computer to be stored, displayed, and sometimes analyzed.

Signal Reconstruction

In many applications, an analog signal is digitized, meaning that successive points on the signal are converted to their digital equivalent and stored in memory. This conversion is performed by an analog-to- digital converter (ADC). A DAC can then be used to convert the stored digitized data back to analog-one point at a time-thereby reconstructing the original signal. This combination of digitizing and reconstruction is

used in digital storage oscilloscopes, audio compact disk systems, anddigital audio and video recording.

Analog-to-Digital Conversion

A analog-to-converter takes an analog input voltage and after a certain amount of time produces a digital output code which represents

An analog-to-digital converter takes an analog input voltage and after a certain amount of time produces a digital output code which represents the analog input. The A/D conversion process is generally more complex and time-consuming than the D/A process. The techniques that are used provide and insight into what factors determine an ADCs performance.

Several important types of ADC utilize a DAC as part of their circuitry. Fig. 7.6 is a general block diagram for this class of ADC. The timing for the operation is provided by the input clock signal. The control unit contains the logic circuitry for generating the proper sequence of operations. The START COMMAND, initiates the conversion process, The op-amp compactor has two analog inputs and a digital output that switches states, depending on which analog input is greater.

The basic operation of ADC.

The basic operation of ADCs of this type consists of the following steps:

1. The START COMMAND pulse initiates the operation.
2. At a rate determined by the clock, the control unit continually modifies the binary number that is stored in the register.
3. The binary number in the register is converted to an analog voltage, V_{AX}, by the DAC.

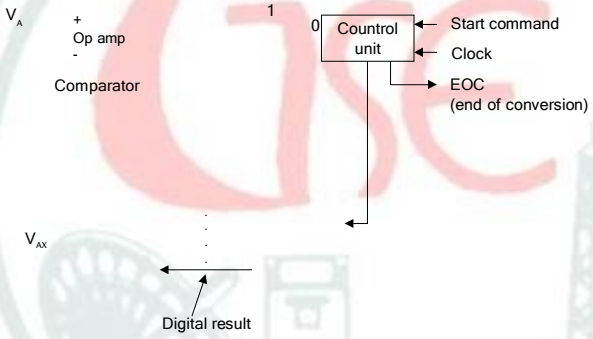


Fig. 7.6 : Basic diagram of ADC.

4. The comparator compares V_{AX} with the analog input V_A. As long as $V_{AX} < V_{A1}$ the comparator output stays HIGH. When V_{AX} exceeds V_A by at least an amount = V_T (threshold voltage), the comparator output goes LOW and stops the process of modifying the register number. At this point, V_{AX} is a close approximation to V_A. The digitalnumber in the register, which is the digital equivalent of V_{AX}, is also the approximate digital equivalent of V_{A1} within the resolution and accuracy of the system.
5. The control logic activates the end-of-conversion signal, EOC, when the conversion is complete.

Digital-Ramp ADC

Operation procedure of adigital-ramp ADC.

One of the simplest versions of the general ADC of Fig. 7.7 uses a binary counter as the register and allows the clock to increment the counter one step at a time until $V_{AX} \geq V_A$. It is called a digital-ramp ADC because the wave form at V_{AX} is a step-by-step ramp (actually a staircase) like the one shown in Fig. 7.7. It is also referred to as a counter-type ADC. Fig. 7.7 is the diagram for a digital-ramp ADC. It contains a counter, a DAC, an analog comparator, and a control AND gate. The comparator output serves as the active-LOW end-of-conversion signal, $\overline{EOC}$. If we assume that V_A, the analog voltage to be converted, is positive, the operation proceeds as follows :

1. A START pulse is applied to reset the counter to zero. The HIGH at START also inhibits clock pulse form passing through the AND gate into the counter.
2. With all 0's at its input, the DAC's output will be V_{AX} = 0V.
3. Since $V_A > V_{AX}$, the comparator output, $\overline{EOC}$, will be HIGH.
4. When START returns LOW, the AND gate is enabled and clockpulses get through to the counter.
5. As the counter advances, the DAC output, V_{AX}, increases one step ata time as shown in Fig. 7.7.
6. This continues unit V_{AX} reaches a step that exceeds V_A by an amountequal to or greater than V_T (typically 10 to 100 μV). At this point, $\overline{EOC}$ will go LOW and inhibit the flow of pulses into the counterand the counter will stop counting.
7. The conversion process is now complete as signaled by the HIGH-to-LOW transition at $\overline{EOC}$, and the contents of the counter are thedigital representation of V_A.
8. The counter will hold the digital value until the next START pulseinitiates a new conversion.

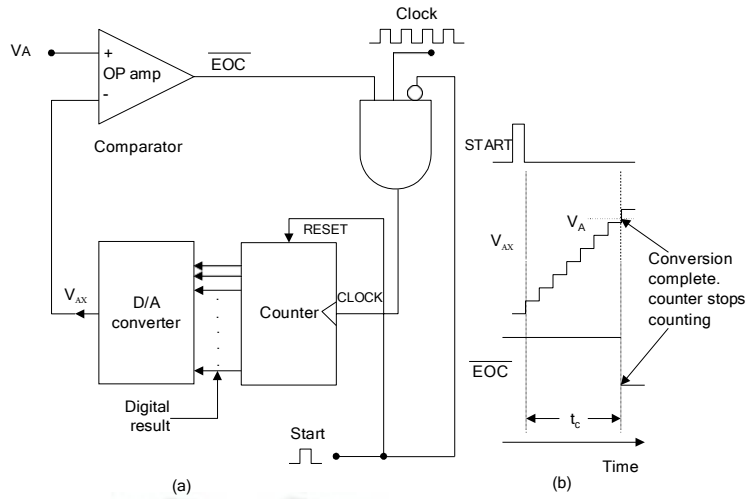


Fig. 7.7 : Digital-ramp ADC.

Problem 8

Assume the following values for the ADC clock frequency = 1 MHz; V_T = 0.1 mV; DAC has F.S. output = 10.23 V and a 10-bit input. Determinethe following values.

Problem 8 and Solution

a. The digital equivalent obtained for V_A = 3.728 V.
b. The conversion time.
c. The resolution of this converter.

Solution

a. The DAC has a 10-bit input and a 10.23-V F.S. output. Thus, the
number of total possible steps is 2^{10} - 1 = 1023, and so the step size is

$$\frac{10.23V}{1023} = 10mV$$

This means that V_{AX} increases in steps of 10 mV as the counter countsup from zero. Since V_A = 3.728 V and V_T = 0.1 mV, V_{AX} has to reach 3.7281 V or more before the comparator switches LOW. This will require.

$$\frac{3.728V}{10mV} = 372.81 = 373\ steps$$

At the end of the conversion, then, the counter will bold the binary equivalent of 373, which is 0101110101. This is the desired digital equivalent of V_A = 3.728 V, as produced by this ADC.

b. Three hundred seventy-three steps were required to complete theconversion. Thus, 373 clock pulses occurred at the rate of one per microsecond. This gives a total conversion time of 373 µs.
c. The resolution of this converter is equal to step size of the DAC, which is 10mV. In percent it is 1/1023 × 100% ≈ 0.1%.

Problem 9

Problem 9 and Solution

For the same ADC of problem 8 determine the approximate range of analog input voltages that will produce the same digital result of $0101110101_2 = 373_{10}$.

Solution

Table 7.2 shows the ideal DAC output voltage, V_{AX}, for several of the steps on and around the 373rd. If V_A is slightly smaller than 3.72 V (by an amount < V_T),

Step	V_{AX} (V)
371	3.71
372	3.72
373	3.73
375	3.75

Table 7.2

Then *EOC* won't go LOW when V_{AX} reaches the 3.72-V step, but willgo LOW on the 3.73-V step. If V_A is slightly smaller than 3.73 V (by an amount < V_T), then $\overline{EOC}$ won't go LOW until V_{AX} reaches the 3.74-Vstep. Thus, as long as V_A is between approximately 3.72 V and 3.73-V, *EOC* will go LOW when V_{AX} reaches the 3.73-V step. The exact rangeof V_A values is

$$3.72\ V - V_T \text{ to } 3.73\ V - V_T$$

but since V_T is so small, we can simply say that the range is approximately 3.72 V to 3.73 V - a range equal to 10 mV, the DAC's resolution.

A/D Resolution and Accuracy

e Resolution of the ADC is qual to the resolution of he DAC that it contains.

Resolution of the ADC is equal to the resolution of the DAC that it contains. The DAC output voltage V_{AX} is a staircase waveform that goes up in discrete steps until it exceeds V_A. Thus, V_{AX} is an approximation to the value of V_A, and the best we can expect is that V_{AX} is within 10 mV

t

of V_A if the resolution (step size) is 10 mV.

Applications

Almost any measurable quantity present as a voltage can be digitized by an A/D converter and displayed. A/D converters are the heart of digital voltmeters and digital MultiMate's. Analog voice signals are converted to digital form for transmission over long distances. At their destination they are reconverted to analog. In digital audio record- the analog audio signal produced by a microphone is digitized (using an ADC), then stored on some medium such as magnetic tope, magnetic disk or optical disk. Later the stored data are played back by sending them to a DAC to reconstruct the analog signal, which is fed to the amplifier and speaker system to produce the recorded sound.

Applications

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Unit-6: LOGIC FAMILIES

OVERVIEW

- **Introduction**
- **Logic Family Classification**
- **Fan IN And Fan Out**
- **Noise Margin**
- **Transistor as a Switch**

- **RTL, DTL, TTL and ECL**
- **Elementary data of CMOS**

Introduction

Logic families represent kind of digital circuit/methodologies for logic expression.

Integration levels :

SSI: Small scale integration — **12 gates/chip**

MSI: Medium scale integration — **100 gates/chip**

LSI: Large scale integration — **1K gates/chip**

VLSI: Very large scale integration — **10K gates/chip**

ULSI: Ultra large scale integration — **100K gates/chip**

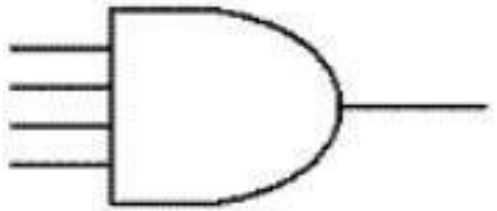
Classification

Logic Family

- Bipolar Logic Family
  - Saturated
    - **RTL(resistor transistor logic)**
    - DCTL(direct coupled transistor logic)IIL(integrated injection logic) **DTL(diode transistor logic)**
    - HTL(high threshold logic)
    - **TTL(transistor transistor logic)**
  - Non Saturated
    - **Schottky TTL**
    - **ECL(emitter coupled logic)**
- ULF(unipolar logic family)
  - PMOS(p-channel MOSFET)
  - NMOS(n-channel MOSFET)
  - CMOS

Fan In

- Fan in or gate is the number of inputs that can practically be supported without degrading practically input voltage level.



Fan in = 4

Fan Out

- The maximum number of digital input that the output of a single logic gate can feed and the gate must be same logic family.

- Fan Out is calculated from the amount of current available in the output ofa gate and the amount of current needed in each input of the connecting gate.

- It is specified by manufacturer and is provided in the data sheet.

Fanout = 4

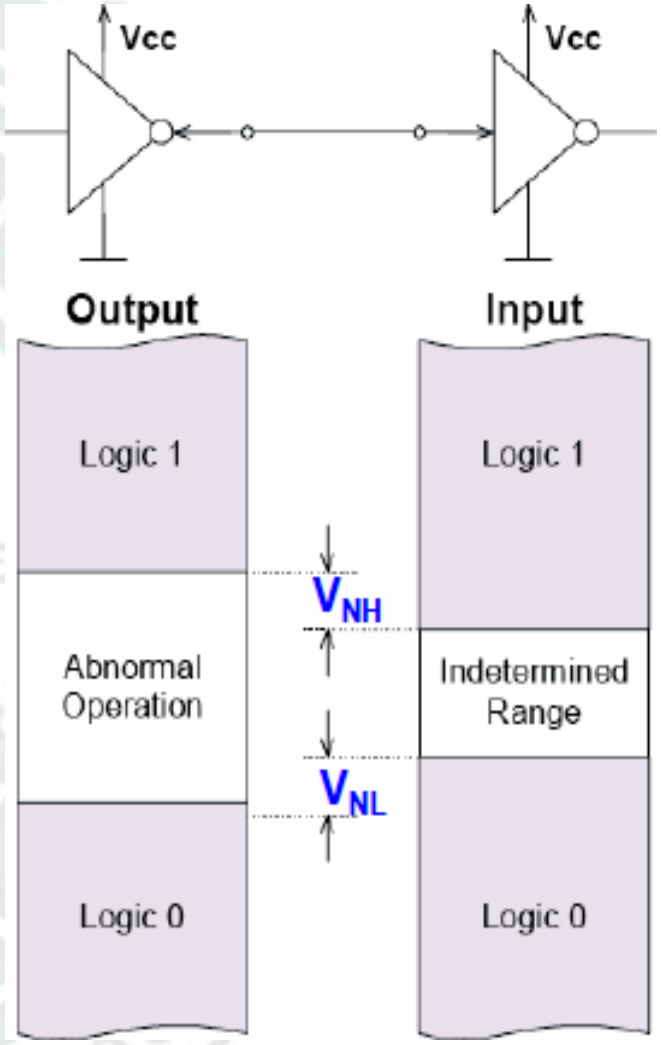
- Exceeding the specified maximum load may cause a malfunction becausethe circuit will not be able supply the demanded power.

Noise Margin

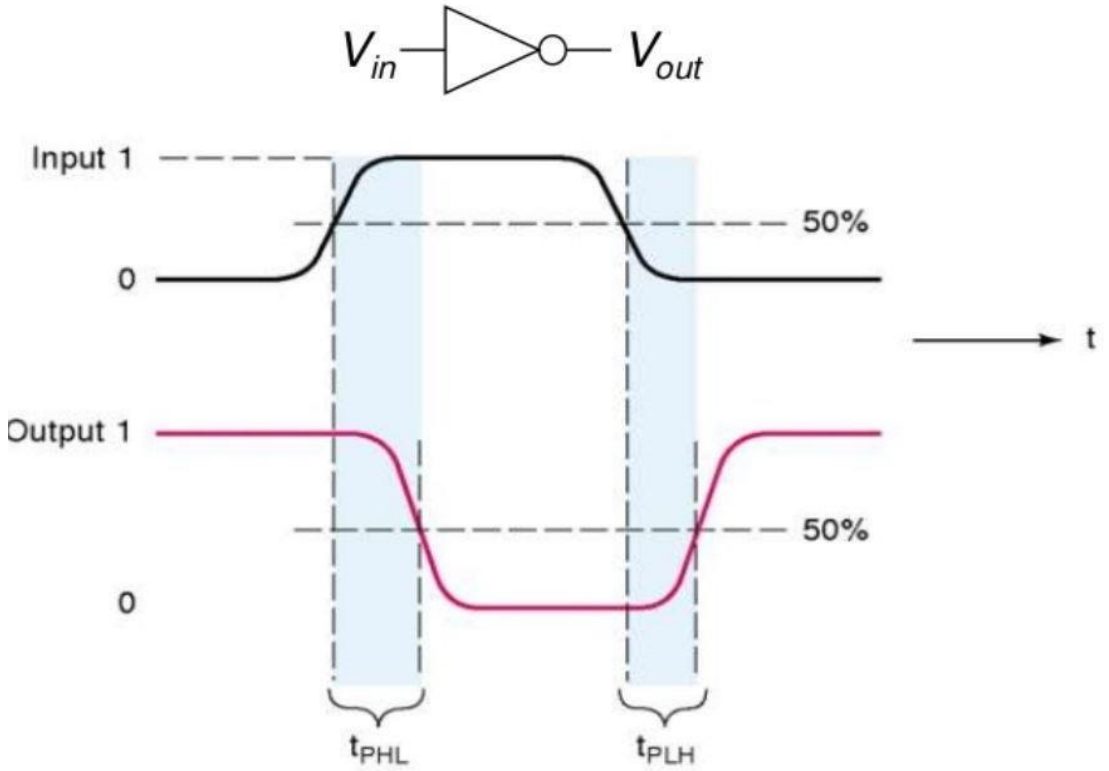
- Noise is present in all real systems. This adds random fluctuations to voltages representing logic levels.

- Hence, the voltage ranges defining the logic levels are more tightly constrained at the output of a gate than at the input.

- Small amounts of noise will not affect the circuit. The maximum noise voltage that can be tolerated by a circuit is termed its **noise immunity (noise Margin).**



Propagation Delay



A measure of how long it takes for a gate to change state. Ideally, should be as short as possible.

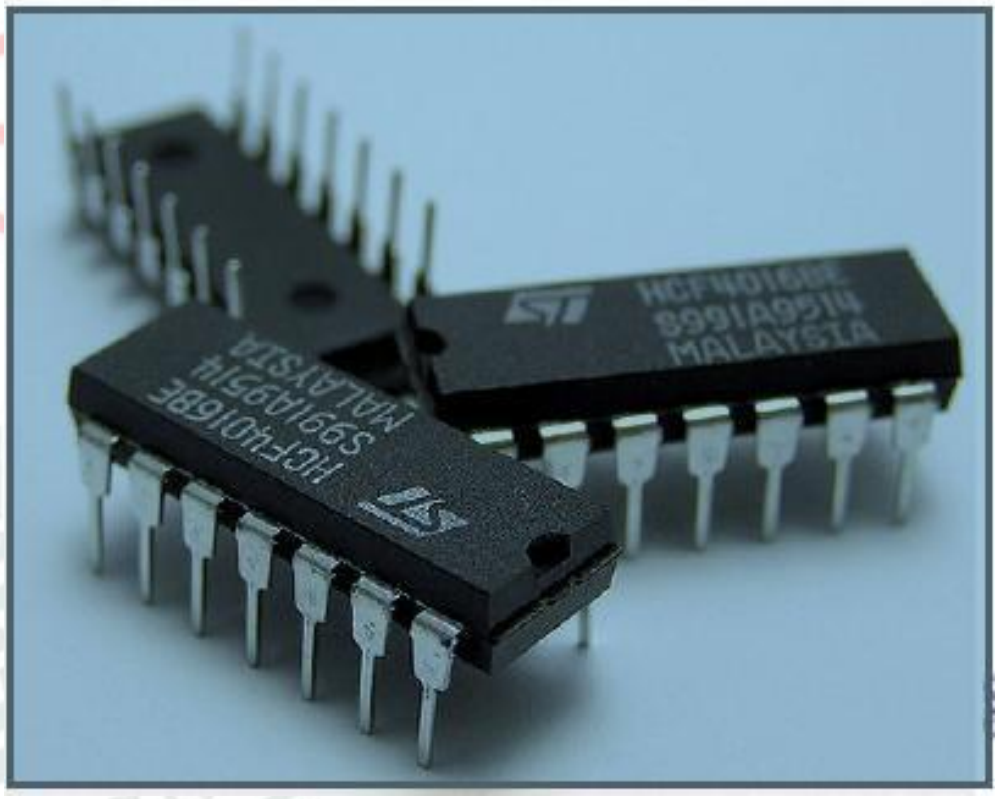
t_{PHL} - the time it takes the output to go from a high to a low

t_{PLH} - the time it takes the output to go from a low to a high

Average Propagation Delay Time $t_p = \frac{t_{pHL} + t_{pLH}}{2}$

Basic Characteristics of ICs

- Propagation delay
- Power dissipation
- Fan in and fan out
- Noise immunity
- Power supply requirement
- Figure of merits i.e. speed power product
- Operating temperature
- Current and voltage parameters



Transistor as a switch

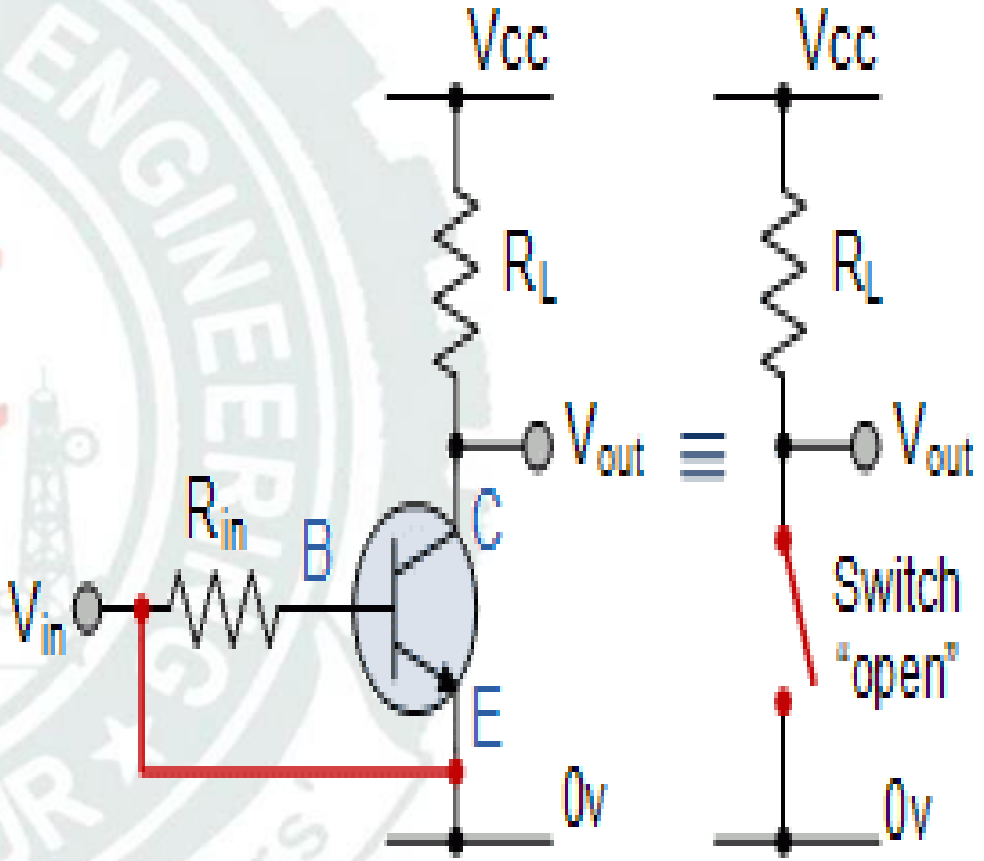
- A circuit that can turn on/off current in electrical circuit is referred to a switchingcircuit and transistor can be employed asan electronic switch.

- Cut off region - OFF State

  Both junctions are reverse biased,Ic = 0 and V(BE) < 0.7 v

- Saturation region - ON State

  Ic = maximum and V(BE)>0.7 v



Resistor Transistor Logic(RTL)

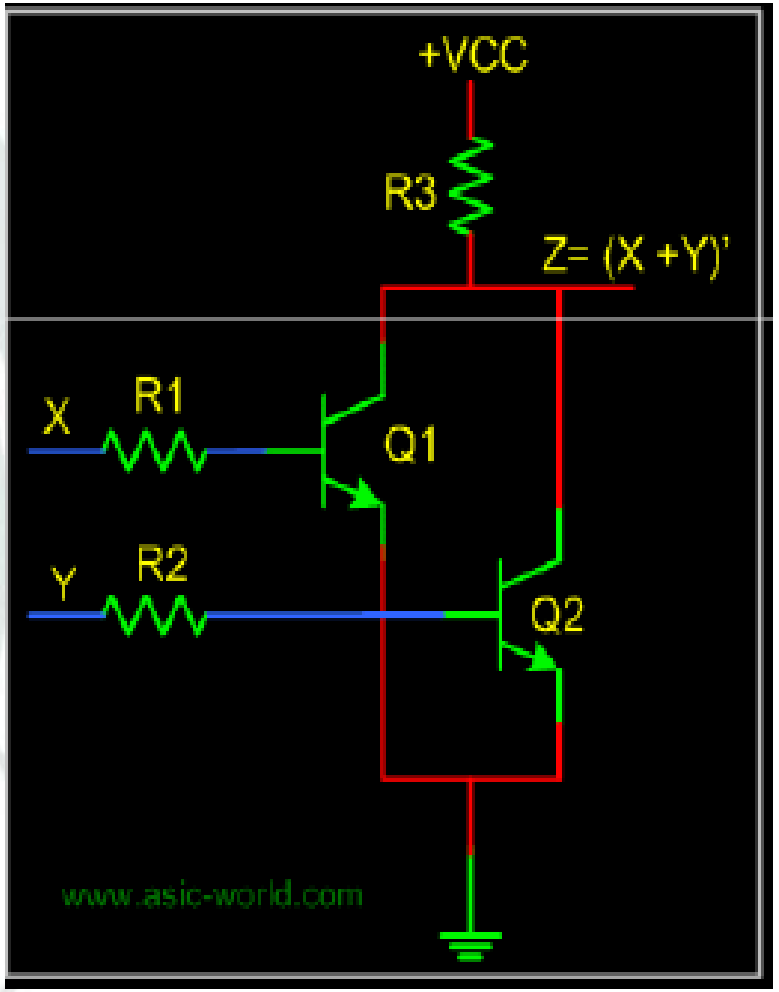
- The basic RTL device is a NOR gate.
- The inputs represent either logic level HIGH (1) or LOW (0).
- The logic level LOW is the voltage that drives corresponding transistor in cut-offregion, while logic level HIGH drives it into saturation region.
- If both the inputs are LOW, then both the transistors are in cut-off i.e. they areturned-off. Thus, voltage Vcc appears at output I.e. HIGH.
- If either transistor or both of them are applied HIGH input, the voltage Vcc dropsacross Rc and output is LOW.

Advantages of RTL Logic circuit:

The primary advantage of RTL technology was that it involved a minimum number of transistors, which was an important consideration before integrated circuit technology, as transistors were the most expensive component to produce

Limitations:

The obvious disadvantage of RTL is its high current dissipation when the transistor conducts to overdrive the output biasing resistor. This requires that more current be supplied to and heat be removed from RTL circuits. In contrast, TTL circuits minimize both of these requirements.



(NOR GATE USING RTL)

Diode Transistor Logic

- The diode-transistor logic, also termed as DTL, replaced RTL family because of greater fan-out capability and more noise margin.
- DTL circuits mainly consists of diodes and transistors that comprises DTL devices.
- The basic DTL device is a NAND gate.
- Two inputs to the gate are applied through diodes viz. D1, D2 . The diode will conduct only whencorresponding input is LOW.
- If any of the diode is conducting i.e. when at least one input is LOW, the voltage at output keepstransistor T in cut-off and subsequently, output of transistor is HIGH. If all inputs are HIGH, all diodes are non-conducting, transistor T is in saturation, and its output is LOW.

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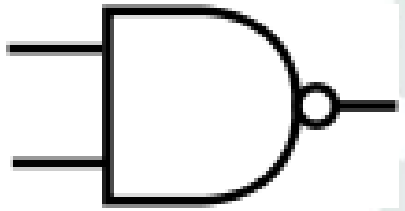
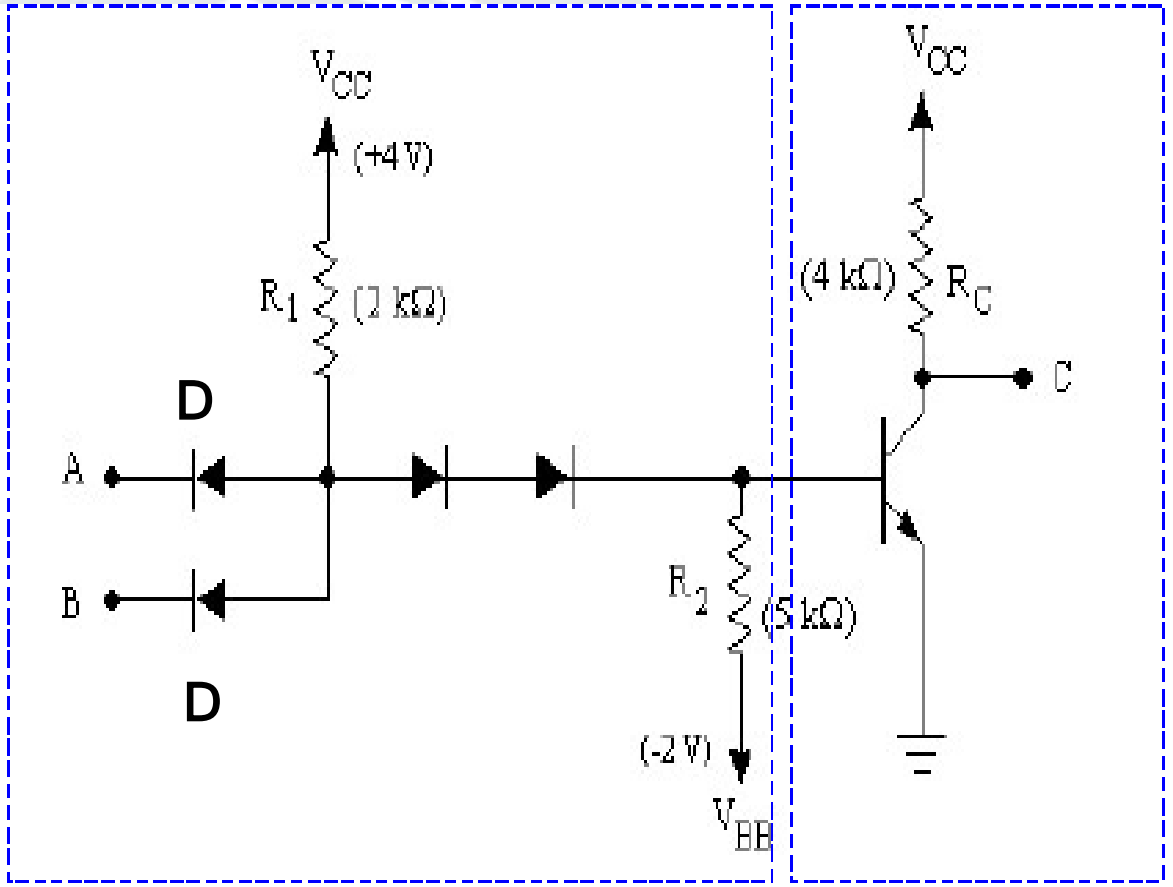
Due to number of diodes used in this circuit, the speed of the circuit is significantly low. Hence this family of logic gates is modified to transistor-transistor logic i.e. TTL family which has been discussed on next slide.





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Transistor Transistor Logic

- TTL family is a modification to the DTL. It has come to existence so as to overcome the speed limitations of DTL family. The basic gate of this family is TTLNAND gate.

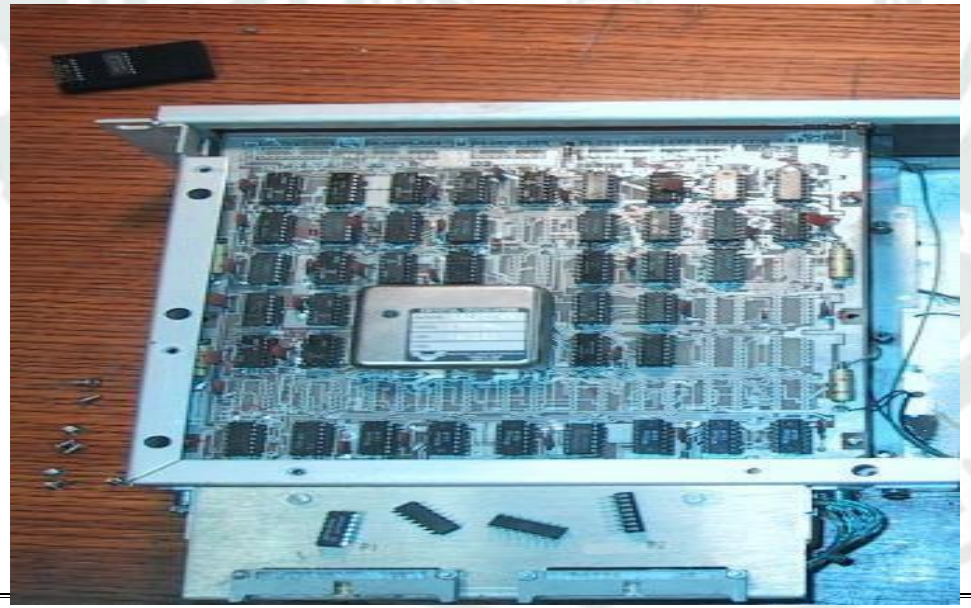
- Q3 is cutoff (act like a high RC) when output transistor Q4 is saturated and Q3 issaturated (act like a low RC) when output transistor Q4 is cutoff . Thus one transistor is ON at one time.

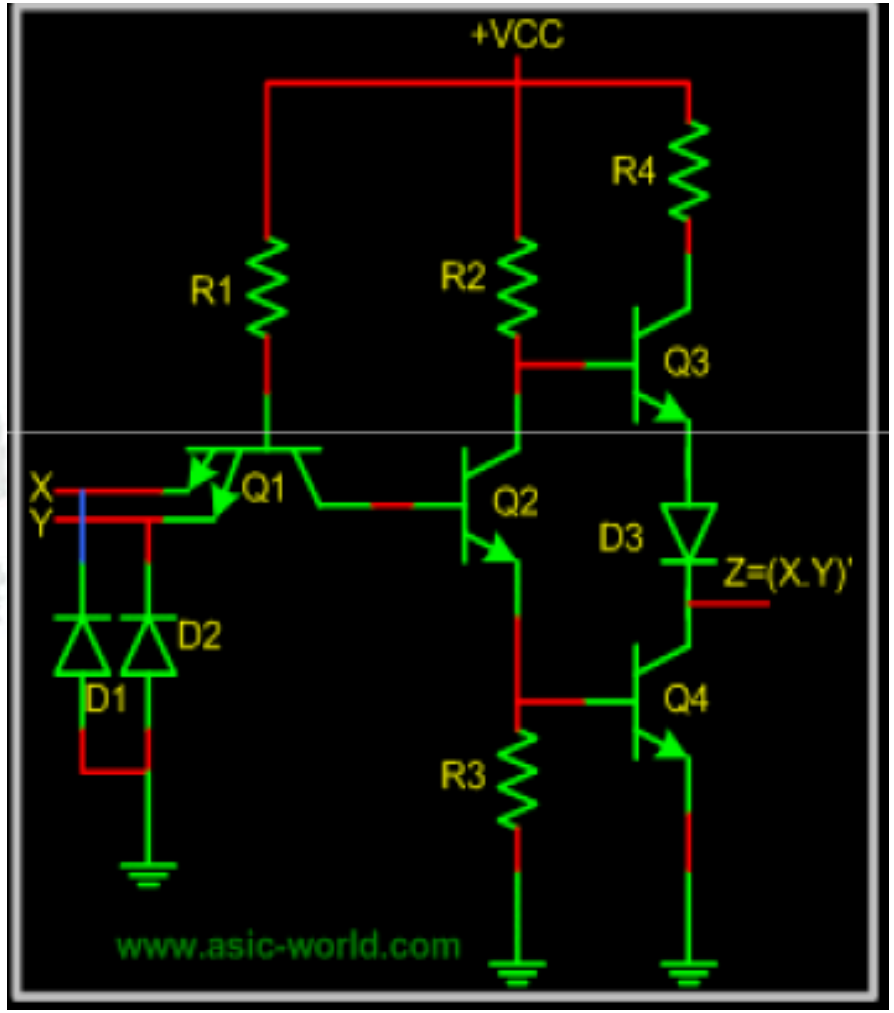
- The combination of Q3 and Q4 is called TOTEM POLE arrangement.

- Q1 is called input transistor, which is multi emitter transistor, that drive transistor Q2 which is used to control Q3 and Q4.

- Diode D1 and D2 are used to protect Q1 from unwanted negative voltages and diode D3 ensures when Q4 is ON, Q3 is OFF.

The output impedance is asymmetrical between the high and low state, making them unsuitable for driving transmission lines. This drawback is usually overcome by buffering the outputs with special line-driver devices where signals need to be sent through cables. ECL, by virtue of its symmetric low-impedance output structure, does not have this drawback.





(BLOCK DIAGRAM OF TTL)

Emitter Coupled Logic

- ECL logic family implements the gates in differential amplifier configuration in which transistors are never driven in the saturation region thereby improving the speed of circuit to a great extent. The ECL family is fastest of all logic families.
- Based on BJT, but removes problems of delay time by preventing the transistorsfrom saturating.
- Very fast operation - propagation delays of 1ns or less.
- Low noise immunity of about 0.2-0.25 V .
- The input impedance is high and the output impedance is low. As a result, the transistors change states quickly, gate delays are low, and the fan out capabilityis high.

(FUNCTION TABLE)

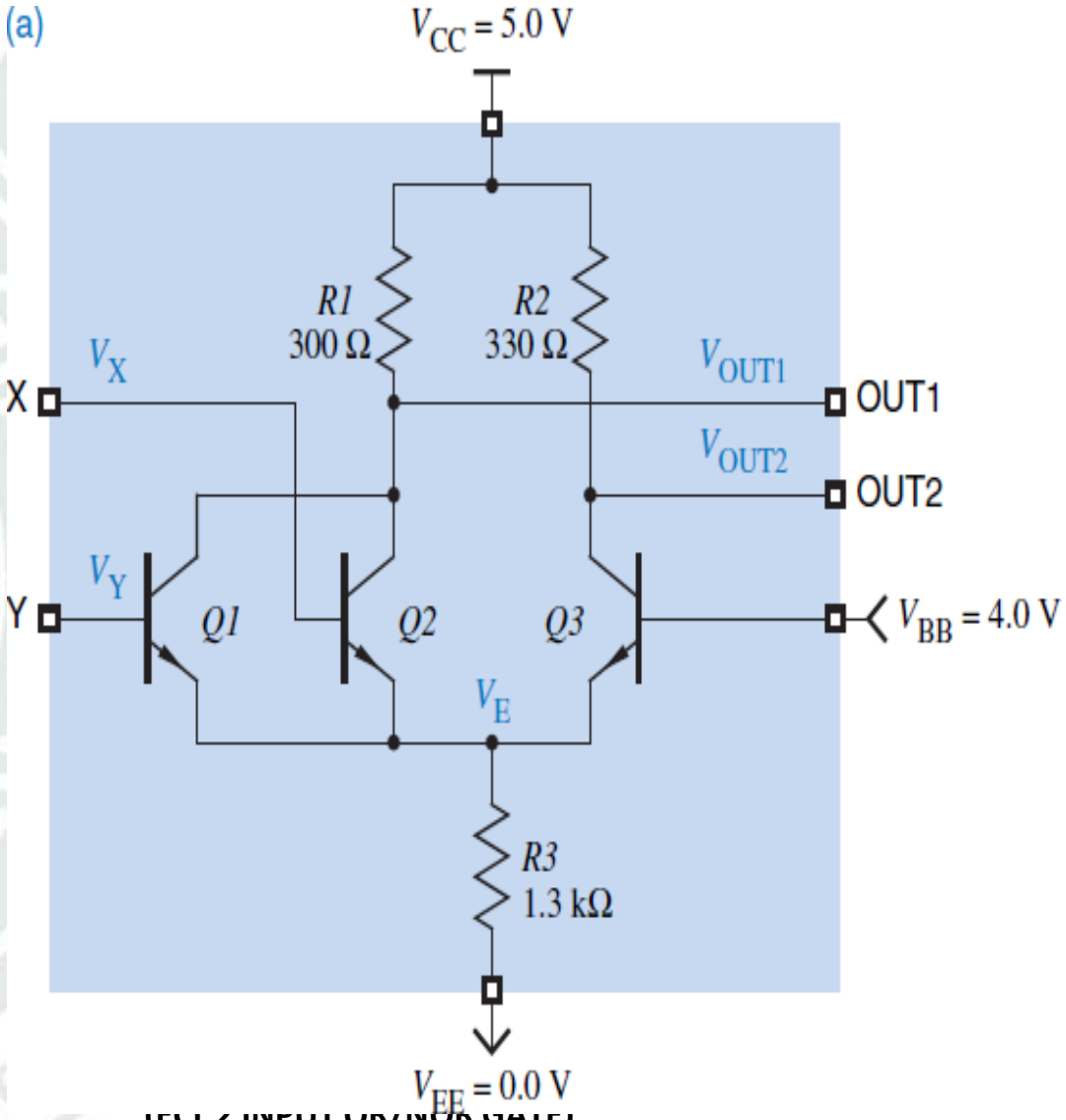
X	Y	V_X	V_Y	Q1	Q2	Q3	V_E	V_{OUT1}	V_{OUT2}	OUT1	OUT2
L	L	3.6	3.6	OFF	OFF	on	3.4	5.0	4.2	H	L
L	H	3.6	4.4	OFF	on	OFF	3.8	4.2	5.0	L	H
H	L	4.4	3.6	on	OFF	OFF	3.8	4.2	5.0	L	H
H	H	4.4	4.4	on	on	OFF	3.8	4.2	5.0	L	H

(TRUTH TABLE)

X	Y	OUT1	OUT2
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

(LOGIC SYMBOL)

(a)



(ECL 2 INPUT OR/NOR GATE)

Complimentary MOS (CMOS)

- Considerably lower energy consumption than TTL and ECL, which hasmade portable electronics possible.
- Most widely used family for large-scale devices
- Combines high speed with low power consumption
- Usually operates from a single supply of 5 – 15 V
- Excellent noise immunity of about 30% of supply voltage
- Can be connected to a large number of gates (about 50) .

Some statistical characteristics data of different logic families

S.N.	Parameter	DTL	HTL	TTL	RTL
1.	Basic Gates (Positive Logic)	NAND	NAND	NAND	NOR
2.	Fan out (Minimum)	8	10	10	5
3.	Typical power dissipation per gate, mW	8-12	55	12-22	12
4.	Noise immunity	Good	Excellent	Very good	Medium
5.	Typical propagation delay/gate, ns	30	90	12-6	12
6.	Clock rate (minimum frequency at which flip-flops operate), MHZ	12-30	4	15-60	8
7.	Number of functions	Fairy High	Medium	Very high	high